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TECHNOLOGY ASSESSMENT AND RADIATION EFFECTS CHARACTERIZATION OF INTEGRATED INJECTION LOGIC

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Integrated Injection Logic (I^2L) has emerged as a bipolar LSI technology which offers high packing density, low power dissipation, reasonable speed and simplicity in processing. In an isolated form I^2L can be incorporated on the same chip with linear devices and/or T^2L or ECL input/output buffering. Another feature of I^2L is the wide range of power and hence speed over which circuits may be operated. The simple double-diffused form of I^2L using lateral pnp transistor injectors has limited speed capability

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which makes it somewhat unattractive for LSI computer applications. Therefore many second generation forms of I^2L have emerged, mainly to increase speed but also to further increase packing density and reduce power. Early radiation effects characterization studies on first generation I^2L indicated that both the neutron and total dose failure levels of I^2L is substantially lower than other bipolar technologies. The changes incorporated into the second generation I^2L processes have, for the most part greatly increased the neutron and total dose failure levels based on test results presented herein. This report presents a technology assessment of I^2L including a discussion of the various second generation processes and commercial product developments by U.S. Companies. An evaluation of radiation effects on first and second generation I^2L is presented along with neutron, total dose and dose rate test results on various I^2L test structures and devices. I^2L is compared to other LSI technologies in terms of packing density, power dissipation, speed, output drive, noise immunity, operating temperature range and power supply requirements. An evaluation of the tradeoffs for radiation hardened I^2L is presented for both first and second generation processes. Military system requirements are discussed for radiation hardened LSI devices.

PREFACE

This report was prepared by the Naval Weapons Support Center, Crane, Indiana under Defense Nuclear Agency MIPR Number 7T-549. The project officer at DNA was Captain Michael V. Bell.

The study began in July 1976 and was completed in September 1976. Section 5 (Comparison of I^2L to Other LSI Technologies) was written by James P. Raymond, Mission Research Corporation, La Jolla, California, who also assisted in discussions with I^2L manufacturers concerning processes and products and with systems project offices concerning military requirements for LSI devices. Mr. Raymond also contributed to the evaluation of radiation effects in I^2L and hardening tradeoffs. The remaining sections were prepared by Ronald L. Pease of Naval Weapons Support Center, Crane, Indiana.

The authors wish to thank Mr. James L. Ramsey and Mr. James C. Wolford for helpful discussions concerning systems application of I^2L, Mr. Richard D. Blice for assistance in evaluations of neutron effects in I^2L, Dr. Young D. Kim for evaluations and measurements of noise immunity and Mr. Gerald L. Hash for assistance in radiation effects measurements.

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SECTION 1

INTRODUCTION

1.1 PURPOSE

This report for the Defense Nuclear Agency by the Naval Weapons Support Center, Crane, and Mission Research Corporation evaluates the integrated injection logic (I^2L) technology for potential hardened military systems applications. The evaluation:

1. Determined what performance and/or cost advantage I^2L has over other LSI technologies that will lead to its use in hardened military systems.
2. Identified the major applications for I^2L in hardened military systems.
3. Characterized the radiation hardness of both first and second generation I^2L.
4. Determined the tradeoffs between hardness and performance for both first and second generation I^2L.

The approach to meeting these objectives was the following:

1. Review the results of the continuing NAVWPNSUPPCEN Crane analysis and characterization program to evaluate the radiation hardness of state-of-the-art I^2L.
2. Survey those companies which have active I^2L programs to determine what products they intend to market, what structures they are using, and what R&D efforts they have to improve the performance and/or hardness of I^2L.
3. Survey military system project offices to determine function, performance and hardness requirements for LSI devices.

In the past two to three years I^2L has emerged as an LSI technology which offers high packing density, low power dissipation, reasonable speed and simplicity in processing. Preliminary radiation effects data on commercial I^2L test structures have indicated, however, that the neutron hardness of I^2L is far less than other bipolar technologies. The primary concern for radiation hardened systems is whether I^2L can be hardened without a substantial loss in performance.

1.2 SUMMARY

In this report an assessment of the I^2L technology is presented in terms of commercial product development, comparisons to other LSI technologies, military system applications, radiation effects characterization and radiation hardening tradeoffs. Development of I^2L for commercial products has been going on in the U.S. for about four years. The largest single use of I^2L to date is in watch chips where all of the electronics, including the LED drivers, is placed on a single chip. This isolated form of I^2L, which allows linear elements to be built on the same chip, can be utilized for many analog/digital applications. Another large market area being addressed by I^2L is the computer chip area. Four I^2L computer chips are on the market and two others are in production. The largest of these is a 7000 gate equivalent 16 bit microprocessor from Texas Instrument. Because of the higher speed requirements for computer chips, most vendors are using second generation forms of I^2L which improve not only speed but fanout, power dissipation and packing density as well. Many commercial I^2L devices are currently under development for single chip controllers, monolithic analog/digital devices, central processing units and other support devices.

Early radiation effects data taken on first generation I^2L structures indicated significant neutron degradation in the 10^{12} - 10^{13} n/cm^2 range and total failure at about 5×10^{13} n/cm^2. These results placed I^2L as the least neutron tolerant of the LSI technologies. However, an anlaysis of causes of the low neutron tolerance and changes in the I^2L structure which might improve it indicated that the higher speed second generation forms of I^2L would have much higher neutron failure levels. Three forms of second generation I^2L have been characterized for neutron effects and have shown improved hardness. Data taken on test structures, such as those used for characterizing first generation I^2L, have indicated neutron failure levels of greater than 3×10^{14} n/cm^2. Modifications of the first generation I^2L structure have yielded neutron tolerances of $1 - 2 \times 10^{14}$ n/cm^2. With the exception of oxide sidewall isolation, the second generation I^2L forms have also demonstrated greater total dose hardness. Test structures of the "advanced" I^2L from T.I., characteristic of the SBP9900, have been tested to 10^7 rad(Si)

and are operational for power dissipation above 1μW per cell. Dose rate upset data on first generation I^2L flip flops has indicated thresholds of $1 - 5 \times 10^9$ rad(Si)/sec for narrow pulse and $10^8 - 10^9$ rad(Si)/sec for wide pulse environments. No latchup has been observed in any I^2L devices and survivability data has been taken at 10^{12} rad(Si)/sec with no catastrophic failures. The radiation performance of the second generation I^2L structures has not been characterized for dose rate effects, transient annealing from neutron pulses or electrical pulse overstress. Also very limited data exists on actual I^2L LSI devices.

The tradeoffs involved in increasing the radiation hardness of either first or second generation I^2L are difficult to access in terms of yield and cost. However, most of the proposed changes to increase hardness involve tighter controls and more processing steps which generally result in lower yield and thus higher cost. On the other hand, in most cases the required changes to increase hardness result in better performance, e.g., higher speed, lower speed-power product and greater packing density. Some exceptions to this are the following:

1. Larger output devices for better drive capability and resistance to electrical pulse overstress (EPO), which result in increased chip area and power dissipation.
2. Use of Schottky T^2L interfaces for noise immunity and EPO tolerance, which requires isolated I^2L and introduces possiblity of latchup.
3. Use of Schottky contacts and clamps to increase speed, which results in lower on-chip noise immunity.
4. Use of oxide sidewall isolation to increase speed, fanout and packing density and reduce photocurrents, which may result in lower total dose tolerance.

In drawing a comparison between I^2L and other LSI technologies many electrical performance parameters as well as packing density, processing complexity, temperature range, power supply requirements, etc., are considered. I^2L is comparable to the best alternative technologies in terms of packing density, dynamic power dissipation, speed power product and operating temperature range but is comparatively weak in terms of noise immunity.

The military system study to determine requirements for radiation hardened LSI devices identified the hardened computer functions as being the largest potential applications area for I^2L. Other areas which might be addressed by I^2L are signal processing, data bussing and A/D, D/A converters. A specific application of I^2L in a military system is the use of the T.I. SPB 9900 16 bit microprocessor in the manpack user equipment for the Global Positioning Satellite system. I^2L was chosen over NMOS because of its greater range of operating temperatures. Other advantages, such as packing density and low speed-power product, are expected to make I^2L attractive for many military applications.

This preliminary study has shown that integrated injection logic is a real, evolving LSI technology of sufficient performance and potential for hardening in support of military systems applications. The present state-of-the-art in I^2L has not yielded sufficient product to judge its commercial acceptance except in the area of watch chips. A broad commercial base for I^2L including computer chips and analog/digital circuits is probable but not obvious. Although I^2L may enjoy a large market in some areas it is unlikely that it will replace any of the existing bipolar and MOS LSI technologies. It will probably not compete in speed with emitter-coupled logic or CMOS/SOS nor will it compare in cost with NMOS or CCDs for large dynamic memories. Application for I^2L seems particularly strong in high density LSI arrays which must operate at moderate continuous clock rates and low chip power dissipation and for circuits requiring both analog and digital functions combined on the same chip.

SECTION 2

I^2L TECHNOLOGY DEVELOPMENT

2.1 BACKGROUND

Integrated Injection Logic (or Merged Transistor Logic) was originally proposed in 1972 by researchers at IBM-Boeblingen for application in a high density, low-power memory[1], and by researchers at Phillips - Eindhoven for application in light-powered instrumentation[2]. Performance characteristics of I^2L arrays were exclusively published by IBM and Phillips through 1974 in several technical papers[3-7]. In 1974, the first papers were published in the design considerations and modeling of I^2L logic cells,[8-11] as well as the first suggestion for performance improvement by process modification (oxide-isolation).[12] Results were presented at the IEEE Electron Device Meeting which examined the sensitivity of the I^2L inverter gain to the characteristics of the n+ isolation collar,[13] and the first major structural variation of the structure (substrate-fed-logic) was proposed as a performance advantage.[14] Early in 1975, Texas Instruments revealed its major development effort in I^2L by the announcement of the SBP 0400 4 Bit Processor Element.[15]

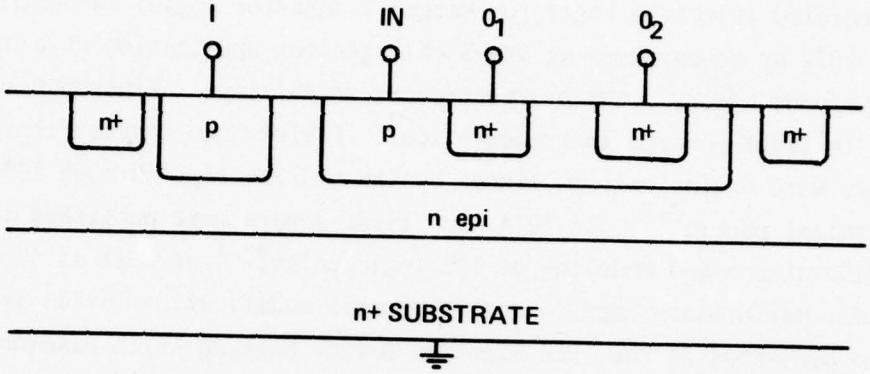
There have been extensive publications on I^2L and its variations from 1975 to the present. These publications generally fall in the categories of:

1. Product design and performance considerations.[17, 25, 26, 31]
2. Variations on the basic structure to improve electrical performance such as the use of Schottky diodes,[16, 21, 27] substrate-fed-logic,[26] vertical injection logic,[32] and folded-collector logic.[33]
3. Modeling and analysis of the baseline I^2L structure.[18, 30, 34]
4. Characterization of radiation effects on available test structures.[19, 23, 24, 28, 36, 37]

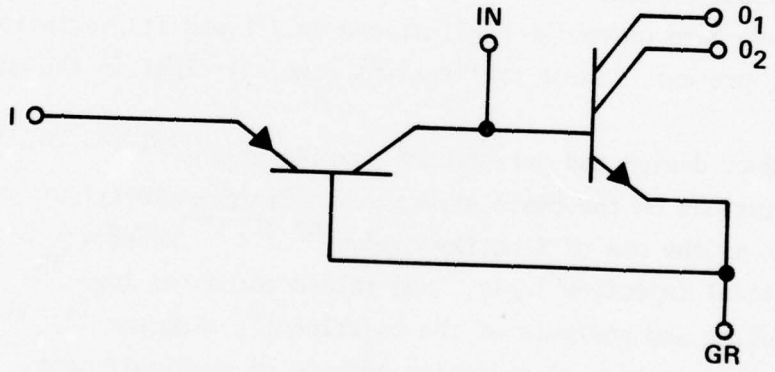
There are also a few papers that provide data in a comparison of competitive LSI technologies,[15, 29, 38] as well as criteria that can be used in comparison.[35] Excluding the earliest papers, most published results on I^2L consider only a digital array rather than as the digital portion of a junction-isolated digital analog array. The process considerations in combined digital/analog arrays are complex,[31] and have so far resulted in but one commercial product.[45]

2.2 DESCRIPTION OF I^2L OPERATION

The basic building block for all I^2L circuits is the inverter cell. A cross section and circuit diagram of a "baseline" commercial I^2L inverter cell is shown in Figure 2.1.



a. Cross Section of 2 Output I^2L Inverter Cell "Baseline" Structure



b. Circuit Diagram of I^2L Inverter Cell

Figure 2.1 Cross Section and Circuit Diagram of I^2L Inverter Cell

High packing density is achieved by operating the small geometry switching transistors in the inverted mode. What are normally emitters are used in I^2L as output collectors (0_1 and 0_2 of Figure 2.1). The epitaxial, normally the collector region, is used as a common grounded emitter (GR). Isolation of the outputs is built in by diffusing the separate collector regions into a common base region which is used for the cell input (IN). Space consuming resistors are eliminated by injecting current into the base region of the switching transistor to provide the necessary bias conditions. The injector (I) is in the form of a lateral pnp transistor which is merged with the vertical inverted npn. The base of the pnp is common to the npn emitter, and the collector of the pnp is common to the npn base. A single current source may be used to bias an I^2L array. Since the forward voltage drop across the injector-to-epitaxial junction determines the largest potential in the circuit, the output voltage in the high state is typically 0.6 - 0.7 volts. This voltage, coupled with the low current operation of the inverted npn (typically 100 nA to 100 μA) gives a power dissipation per gate of tens of nW to tens of μW.

The critical parameters for the operation of the inverter cell are the propagation delay, the current gain of the lateral pnp transistor and the current gain of the npn transistor. The propagation delay at low injection is dominated by the emitter-base depletion capacitance of the npn transistor and varies inversely as the npn emitter current. As the current increases the active hole charge stored in the epitaxial layer becomes larger than the npn depletion layer stored charge and the delay becomes independent of current.[18] At high injection the lateral base resistance prevents rapid charging and discharging of the active region and the delay increases with current. The current gain of the lateral pnp transistor is best expressed by the common base current gain α. Alpha is a direct measure of the amount of hole current available to the base of the npn to satisfy recombination and thus establishes the operating current for the npn. The common emitter current gain of the npn (βu) is a measure of the amount of base current a collector can sink, or the fanout per collector. Since in most I^2L circuit designs a collector sinks no more than one base, the requirement for operation is that at the βu per collector be greater than one. The one exception is substrate fed logic where the amount of base current that a collector must sink is proportional to the base area being driven. The fanout per collector requirement in this case is the ratio of base areas. If multiple inverter cell fanout is required (normally the case for random logic arrays), then multiple collectors are used. Typical cell fanout is 3-5.

2.3 DETAILS OF VARIOUS I^2L FORMS

Many forms of I^2L have been proposed to increase speed and packing density and lower power dissipation. The general categories of I^2L are the following:

1. Diffused first generation
2. Ion-implanted
3. Up-diffused
4. p epitaxial
5. Substrate fed

The actual variations of I^2L involve not only these basic approaches but also various forms of oxide isolation, Schottky contacts (base and collector), Schottky clamps (collector-base) and many different injector forms. In the following paragraphs, details of I^2L structures in current use, as well as proposed structures will be given.

2.3.1 Non-isolated First Generation I^2L

The non-isolated "baseline" or first generation form of I^2L was shown in Figure 2.1. The emitter of the npn as well as the base of the lateral pnp consists of an n-type epitaxial layer grown on an n+ substrate. A p diffusion into the n epitaxial forms the emitter and collector region of the lateral pnp as well as the base of the npn (coincident with the pnp collector). A final n+ diffusion forms the collectors of the npn transistors as well as the guard ring around the npn base region. Guard rings reduce lateral injection from the npn base region improving the npn up gain. With no gap between the n+ guard ring and the p base region the emitter base depletion capacitance is increased which reduces speed at low injector currents. Therefore, some vendors prefer to leave a small gap between these diffusions. Further improvements in gain can be realized by performing a separate deep n+ diffusion to form the guard ring. This, however, requires a separate mask and diffusion step.

2.3.2 Junction Isolated First Generation I^2L

The junction isolated first generation structure is shown in Figure 2.2.

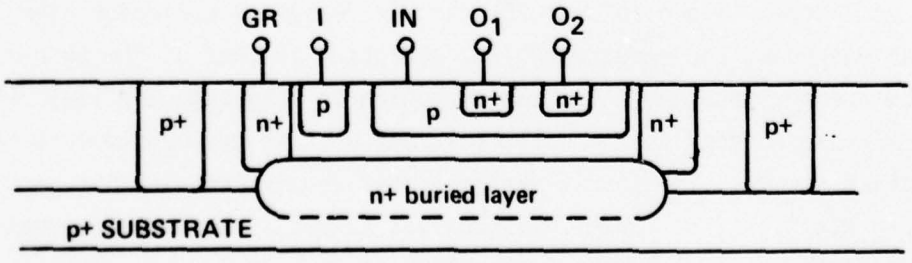


Figure 2.2 Cross Section of Junction Isolated First Generation I^2L Inverter Cell

In this structure a buried n+ layer is formed on a p+ substrate which partially up-diffuses through an n epitaxial layer. A p diffusion forms the injector and npn base region, and an n+ diffusion defines the npn collectors. Contact to the n epi and buried layer (npn emitter) is made with a deep n+ diffusion, which also serves as a guard ring. Although the guard ring and ground contact can be made coincident with the npn collectors, a separate deeper n+ diffusion improves the npn up gain. Isolation of the I^2L cells is achieved by deep p+ diffusions extending through the epi. This structure is compatible with linear processing and is used for devices requiring both digital and linear circuits on the same chip. It may also be used where on-chip LST^2L or ECL buffers are required.

2.3.3 Ion-Implanted I^2L

In order to improve the npn base doping profile, concentrate current flow in the intrinsic base region (region immediately under the npn collectors), and provide better control of the intrinsic base width, many vendors are using an ion-implanted base structure for I^2L. Although the ion-implanted base is common to this structure, there are several variations being used. The first product on the market using this approach is the Fairchild 9408. This structure[56] is shown in Figure 2.3.

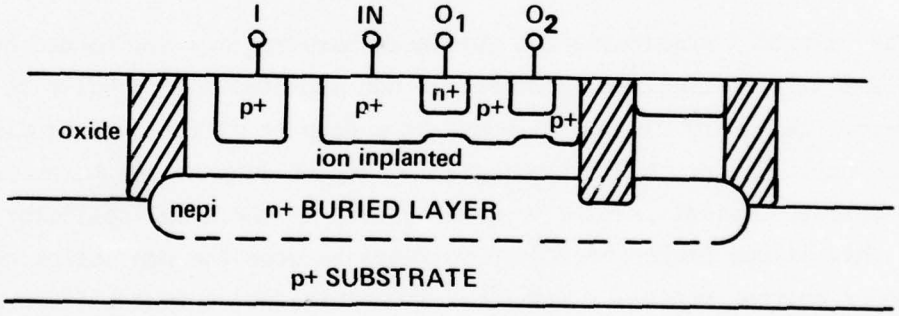


Figure 2.3 Cross Section of Fairchild Isoplanar, Ion-Implanted I^2L Inverter Cell

A high energy boron implant into the thin epitaxial layer defines the npn intrinsic base regions. The injector and extrinsic npn bases are formed by a highly doped p diffusion which improves the gain of the lateral pnp and

helps concentrate npn current flow in the intrinsic base region. An n+ diffusion forms the npn collectors and the ground contact to the npn emitters. The structure shown in Figure 2.3 is an isolated form of I^2L built on a p substrate allowing fabrication of T^2L circuits on the same chip. The isolation is Fairchild's Isoplanar process. This sidewall isolation also inhibits lateral hole injection from the p+ regions and reduces the npn emitter-base depletion capacitance.

Another form of ion-implanted I^2L (T.I.'s "advanced" I^2L used on the SBP9900 microprocessor) is shown in Figure 2.4.

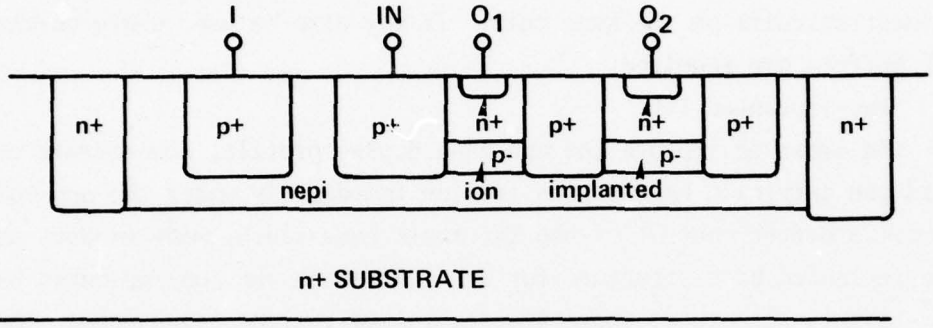


Figure 2.4 Cross Section of Texas Instrument Ion-Implanted I^2L Inverter Cell

As with the Fairchild structure, the intrinsic base regions are formed by a deep boron implant. This structure, however, is non-isolated and is built on an n+ substrate. The guard rings are formed by a deep n+ diffusion extending through the epi. Rather than diffusing an n+ region down to the boron implant, a shallow arsenic implant is used to make contact to the n epi collector regions. This allows higher breakdown voltages between the npn collector-base and collector-emitter regions. With this structure, the output buffers are open collector I^2L transistors.

Another form of ion-implanted I^2L is described by Bell Telephone Labs.[57] This structure is essentially the same as shown in Figure 2.4 except contact to the n epi collector regions is made with Schottky contacts rather than a shallow n+ implant. Schottky collectors reduce the output voltage swing and thus increase switching speed.

Although Fairchild, TI and BTL are the only U.S. companies that have produced devices using ion-implanted I^2L, several other companies are working with similar ion-implanted structures. These include RCA, Northrop and Signetics.

2.3.4 *Up-diffused* I^2L

The first I^2L work published using an up-diffused p region was that of ITT semiconductors.[47] This structure is shown in Figure 2.5. The npn base and injector regions are formed by depositing boron on an n+ substrate. An n epitaxial layer is grown and the boron is subsequently out-diffused. Collectors are formed by diffusing n+ regions. The individual cells are isolated by the formation of anodized oxide. ITT has developed a special technique to form deep anodic isolation.

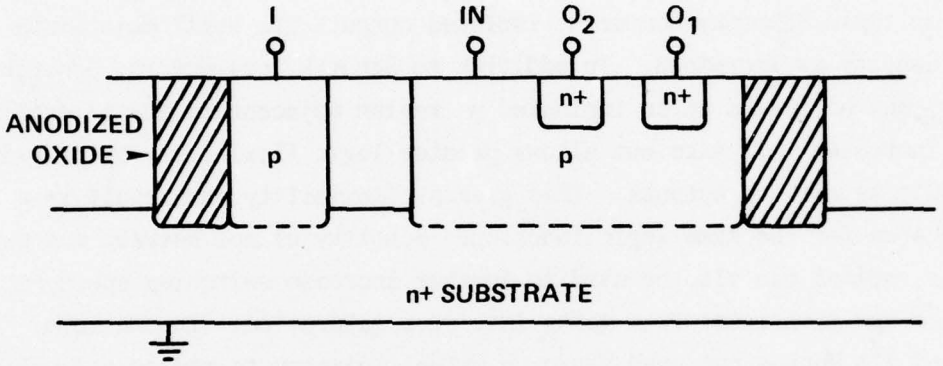


Figure 2.5 Cross Section of ITT Up-diffused I^2L Inverter Cell

Using an up-diffused base region reverses the doping gradient in the intrinsic base region from that of down-diffused structures. This provides an aiding rather than a retarding base electric field for the inverted npn, thus increasing up gain.

A structure similar to this is used by Hughes semiconductor[49] to achieve very high up gains. The Hughes up-diffused structure is shown in Figure 2.6.

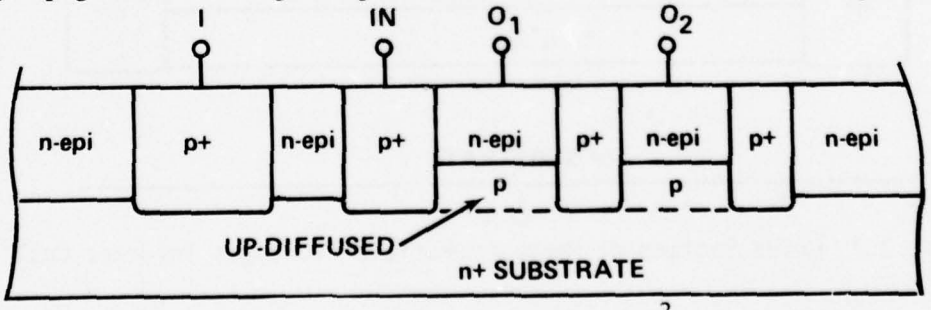


Figure 2.6 Cross Section of Hughes Up-diffused I^2L Inverter Cell

In this process, boron is implanted on an n+ substrate and partially up-diffused through the n epitaxial layer as it is grown. P+ diffusions form the injector and extrinsic npn base regions. The up-diffused intrinsic base has a steep doping profile which is in the proper direction for the inverted npn transistor. The collector region of the npn is the n epitaxy which provides reasonably high breakdown voltages. A shallow n+ diffusion forms the contacts to the collector regions and the guard ring.

Hughes has worked with many variations of this basic structure. As with the ion-implanted structure, Schottky contacts may be made at the collector regions. This not only provides an increase in switching speed but also allows the removal of the p+ diffusions between collectors in the same cell. By using a single collector region with multiple Schottky contacts, isolated outputs are still maintained and packing density is increased. In addition to Schottky collectors, Schottky base contacts may be formed on an implanted p- region adjacent to the p+ extrinsic base. This increases cell size but allows greater logic flexibility by providing multiple inputs as well as outputs. This greater flexibility can result in a reduced chip area for the same logic function. Schottky clamps between the base and collector regions can also be used to further increase switching speed by preventing the npn transistor from going into deep saturation. In one form of up-diffused I^2L Hughes has used V-groove oxide isolation to reduce sidewall injection and depletion capacitance.

2.3.5 Substrate Fed Logic

Substrate Fed Logic (SFL) was first introduced by Plessy of England.[14,20] Although it has been tried by a few U.S. companies, it is only being actively pursued by Harris Semiconductor.[36] A cross section of the Harris SFL is shown in Figure 2.7.

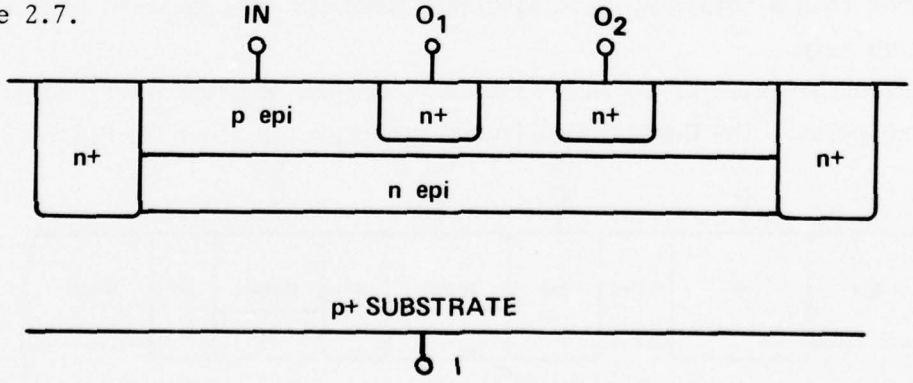


Figure 2.7 Cross Section of Harris Substrate Fed Logic Inverter Cell

In this form of I^2L the p+ substrate is used as the injector. A thin n epitaxial layer is grown on the p substrate to form the pnp base and npn emitter region. A thin p epitaxial layer is grown on the n epi to form the pnp collector and npn base. A deep n+ diffusion isolates the inverter cells and provides contact to the ground plane. A final n+ diffusion forms the npn collectors. As with other I^2L structures, oxide sidewalls may be used to isolate the I^2L circuits from the input/output buffering. The ground contacts are made on the top surface.

2.3.6 P Epitaxial I^2L

ITT proposed one of the first p epitaxial structures.[47] In this structure, shown in Figure 2.8, a low concentration phosphorus region is diffused into an n+ arsenic doped substrate. A p epi is grown and the phorphorus is up-diffused through the p epi to form the pnp bases and inverter cell isolation.

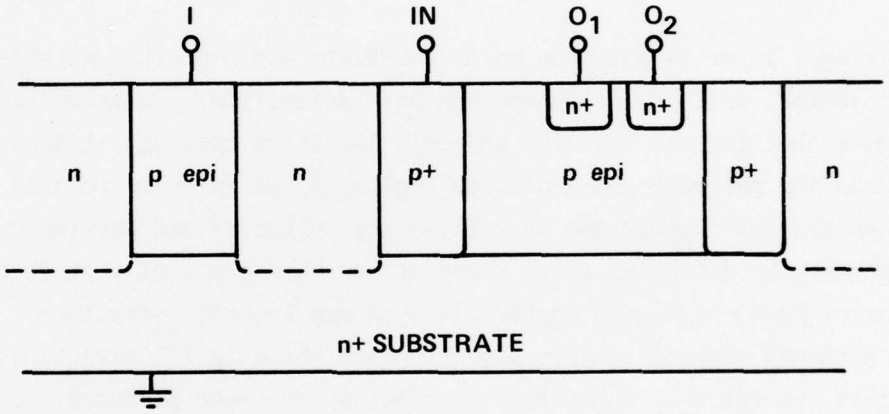


Figure 2.8 Cross Section of ITT p Epitaxial I^2L

A deep p+ diffusion forms a portion of the npn extrinsic base region, and a final n+ diffusion forms the npn collectors.

Another approach to p epi I^2L is shown in Figure 2.9.

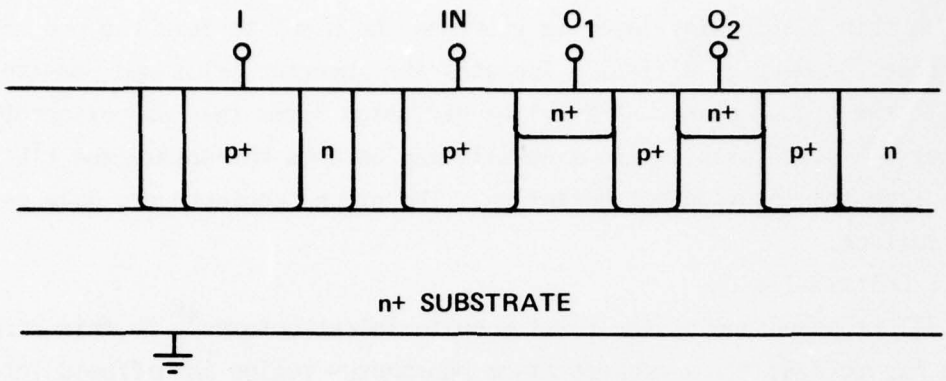


Figure 2.9 Cross Section of Proposed p Epitaxial I^2L Inverter Cell

A thin p epitaxial layer is grown on an n+ substrate and deposited nitride is etched for injector, cell isolation and npn base definition. An oxide layer is deposited and etched for the injector and cell isolation opening. A deep n diffusion forms the pnp base and isolation regions. The oxide is removed and a p+ diffusion through the nitride mask forms the injectors and extrinsic npn base regions. By diffusing first n dopant and then p dopant through the same opening a narrow base, high gain double diffused pnp injector structure is formed. Although several vendors have proposed building I^2L structures similar to this, so far only laboratory test chips have been produced. Companies which have worked with this structure include RCA, T.I. and Northrop. As will be discussed in Section 2.4.2, Fairchild uses an Isoplanar structure very similar to that of Figure 2.9 in their 4K dynamic RAM. However, it is not operated as a conventional I^2L array.

2.4 COMMERCIAL I^2L DEVELOPMENTS BY U.S. COMPANIES

Since the major concern for military applications of I^2L will be developments by U.S. companies the technology assessment of I^2L performed in this study did not address foreign development. The major companies which have active I^2L programs for the development of commercial products are T.I., Fairchild, Motorola, Signetics, ITT and RCA. Several other U.S. companies have I^2L programs, supported primarily by IR&D money, which are directed toward development of I^2L for military systems applications. Among these are Northrop, General Electric, Hughes, Boeing, Harris Semiconductor and Westinghouse. This list is not comprehensive but does include the known major efforts. Many of the companies mentioned were surveyed in this study to acertain the following information regarding their I^2L program.

1. How big is the I^2L effort, how long has it been going on and how is it funded?
2. What I^2L products does the company have on the commercial market and how many devices are in production?
3. How many and what type of devices are in pilot production or design?
4. What is the cell structure of the devices in production and what is being done to improve the performance of future product (speed, power, drive capability, packing density, etc.)?
5. What are the design layout rules for I^2L and does the company have a standard cell library for computer aided design?
6. What considerations have been given to radiation effects and how much interest does the company have in military applications?

The surveys were conducted both by personal contact and through the use of questionnaires. The results of the survey are presented by a discussion of each company's program. Because commercial interest and radiation hardened military interest were both addressed in the surveys, the results of both efforts will be presented. The semiconductor vendors surveyed in this study whose primary interests are in commercial I^2L products were Fairchild, ITT, T.I., Motorola, RCA, Signetics and National. Companies having interests primarily in military I^2L products which were surveyed in this study were Northrop, G.E., Harris and Hughes.

2.4.1 Texas Instruments

One of the largest efforts in the U.S. in I^2L technology has been at Texas Instruments. There are currently 15-20 people at T.I. working on I^2L. The first and largest (in terms of sales) product development by T.I. was a watch chip. Built with an isolated version of the "baseline" I^2L process, everything but the LEDs, battery and a trim capacitor are placed on one chip. Using this process, T.I. has developed LSI chips for teletype systems, cameras, T.V. circuitry, and other consumer products.

In 1974, T.I. announced a 4 bit parallel binary processor element, the SBP0400 using non-isolated "baseline" I^2L. This device has limited applications, because of the operation propagation delay times of 100-530 nsec (at nominal power). This "baseline" I^2L structure has been characterized for neutron, long-term ionization, and dose rate response.[19, 20, 32]

In order to improve the speed of I^2L to make it competitive for LSI level computer applications, T.I. developed what they refer to as "advanced" I^2L. The advanced I^2L process, shown in figure 2.4 utilizes thin epitaxy and ion implantation. This process has yielded minimum prop delays of 4-5 nsec on ring oscillator test devices as compared to the 20-30 nsec measured on "baseline" I^2L.

The first major product announcement by T.I. using "advanced" I^2L is the SBP9900 16 bit microprocessor. The development of the I^2L version of the 9900 was supported in part by the Air Force Space and Missile System Organization (SAMSO) through a T.I. Systems group which will use the part in a prototype version of the manpack user equipment for the Global Positioning Satellite (GPS) System. The 9900 was first designed and fabricated in N-MOS having the notation TMS 9900. In order to use the 9900 in the GPS user equipment, the T.I. systems group needed a full Military temperature range part, hence the development of the SBP9900 in I^2L. A comparison of the two parts is given in Table 2.1.

TABLE 2.1 COMPARISON OF T.I. TMS9900 AND SBP9900

	SBP9900 (I^2L)	TMS9900 (n-MOS)
Power Dissipation	500mW at 2MHz	650mW at 3MHz
Clock Requirement	Simple phase static	4 Phase dynamic
Power Supplies	One current supply	+5, -5V, +12V
Clock Rate	Variable from DC to 2MHz	3MHz fixed
Operating Temp Range	-55 to +125°C	0 to +70°C

T.I. will use the "advanced" I^2L technology to produce peripheral chips to be used with the 9900 in addition to memories. In 1977 they plan to market a 4K Static RAM, the SN54S400 which utilizes isolated "advanced" I^2L for the memory matrix and low power Schottky T^2L for the remaining circuitry. The advance data sheets claim 75ns read cycle and 75ns write cycle times. The design goals were released for this part in July 1976.

T.I. has shown much interest in radiation hardened I^2L, but has not initiated the development of hardened arrays. They have made proposals to various DOD program offices to initiate a hardening effort using a p epitaxial structure. This structure shown in figure 2.9, may offer improved speed as well as improved neutron and total dose hardness because of the high gain injector structure and improved npn profile. So far this effort has not been funded by DOD.

Recent tests by NAVWPNSUPPCEN Crane on "advanced" I^2L test structures indicate a significant improvement in the radiation hardness of this structure over the "baseline" structure. Based on this data (presented in a later section), T.I. feels that their "advanced" I^2L will meet most system hardening requirements but still thinks another structure, such as p epitaxial, will be required to meet very high neutron fluence levels.

2.4.2 Fairchild

Fairchild has been developing Isoplanar I^2L for about four years on IR&D funding for application in the computer and memory area. They have announced two I^2L products, the 9408 Microprogram Sequencer and the 93481 4K X 1 dynamic RAM. They have two additional circuits under development, the 9412 CRT controller and 9423 First In First Out Memory (F1F0) which they hope

to market in the first quarter of 1977. Their most recent announcement[50] is a one-chip emulation of the Nova 1200 minicomputer's central processing unit. It is faster and 32% smaller than the N-MOS CPU built by Data General for its microNova.

Both the 9408 and 93481 are Isoplanar structures; however, the 9408 utilizes an n epitaxial with ion implantation shown in figure 2.3, whereas the 93481 is built on a p epitaxial and uses a double diffused pnp which provides high frequency operation. The 93481 is not a conventional I^2L array, although the cell resembles the I^2L structure shown in Figure 2.9. The emitter of the pnp, rather than being used simply as an injector, is used as a word line. The collector of the npn is also a word line and the npn emitter is the bit line.[46] The logic level is determined by the charge on the collector-base junction of the npn transistor. By utilizing both the pnp and npn transistors as switches and operating dynamically, one single merged inverter cell serves as a memory element.

The performance characteristics of Fairchild's Isoplanar I^2L (I^3L) are as follows:

1. Minimum propagation delay.
   2.5 nsec at 1-2mA on test structures.
   5nSec at 0.2mA in selected product.
2. Minimum speed power product.
   .015 pJ in test structures, .15 pJ in logic product.
3. Drive capability.
   16 mA using T^2L - like output buffers of totempole structure.
4. Maximum packaging density.
   600 gates/mm^2 in high density areas of chip.

Fairchild plans future additions to their macrologic family and more advanced dynamic and static memories. They have a standard cell library for computer aided design.

2.4.3 Motorola

Motorola has been involved in high density bipolar technology for 3-4 years. In 1974-75 they were working on Complementary Current Controlled Logic C^3L which involves a very sophisticated Schottky process. This work was dropped and I^2L was considered for the computer memory and pheripheral area.

In January 1976 Motorola announced development of a megalogic family of I^2L parts for interfacing with the 6800 microprocessor family.[51] These circuits included a floppy disc generator, programmable delay module, 8 X 8 multiplier, and parity interrupt controllers. Later they announced that they had dropped work in I^2L for the memory and microprocessor area.[52] The effort at Motorola in I^2L is now in the combined analog/digital area. At present they have one device in production which is used as an organ divider circuit. They have 8-10 devices in pilot production and another six in design, all using the junction isolated "baseline" I^2L combined with analog circuitry. They are aiming at the communications/telephone and control circuitry markets.

2.4.4 Signetics

The major effort in I^2L at Signetics has been in the computer area. Signetics is developing a family of computer peripheral circuits to be used with their 8 bit microprocessor. They have two devices in production at this time, a Cyclic Redundancy Character Generator/Checker (150 gates with max clock of 10MHz) with part number 8X01 and a First In First Out Memory (FIFO) (550 gates with max clock of 10MHz) with part number 8X04. Both of these circuits utilize the "baseline" I^2L process and the 8X04 has LST^2L inputs and outputs. They have several I^2L devices in the development stage: a direct Memory Access Control Unit, a 64 X 8 FIFO, 16 X 8 LIFO, a multiplier and a peripheral interface unit. The FIFO is 3000 gate complexity and will operate at 10MHz. In the R&D area Signetics is working on high speed I^2L using ion implantation. All of their high density I^2L devices will have dual level metal so that injector rails will have sufficiently low resistance to avoid significant IR drops at the higher speeds. They feel that two levels of metallization will be necessary for all high density I^2L devices. A rather innovative area being pursued by Signetics using I^2L is the concept of multiple level logic. At present they are working with four level logic. The levels are represented by incremental currents which are controlled by the output transistor geometry and biases. Such a concept can be used to significantly reduce the external pin count required for LSI level devices.[48] This concept of four level logic has been used in the 8X04 FIFO. Although the inputs and outputs are binary, multilevel weighted summing and detection schemes are used internally. A significant reduction in the number of necessary transistors was achieved in this design.

2.4.5 RCA

The efforts at RCA in I^2L have been directed toward three market areas. The first area is that of combining digital I^2L functions with analog devices on the same chip. RCA has one such circuit, used in a digital panel meter produced by Analog Devices in production.[45] The form of I^2L used is the junction isolated "baseline" I^2L process as shown in figure 2.2. The second market area is that of timekeeping. RCA's effort here is directed toward extending I^2L to very low current ranges to cut power consumption. They have two watch circuits in the design phase and expect production by mid-1977. The third area of interest is the computer area. This effort is directed toward increasing the speed of I^2L. The two approaches being taken are the following:

1. A thinner epitaxial, ion implantation for the base and collector of the npn, and oxide sidewall isolation (similar to figure 2.3).
2. A thin p epitaxial on n+ substrate with a double diffused injector structure (similar to Figure 2.9).

The high speed I^2L structures used for the computer circuits are of interest for military markets because of the greater expected neutron hardness. They propose design of a microprocessor, a 1K RAM and possible peripheral circuits. At present they are processing ion-implanted test chips and expect to process p epi structure by mid-1977.

2.4.6 ITT

ITT has been working with the I^2L technology for about 3-4 years. Their only production circuits are watch and watch-calculator interface chips using the "baseline" structure. Unlike most company approaches to I^2L, ITT feels there is a place for I^2L at the MSI level. They have three MSI level circuits including the 54191 (up-down counter) in development which will be used as replacements for the low power Schottky T^2L series. The anticipated production for these circuits is second quarter 1977. ITT intends to qualify these parts to the MIL-M-38510 specification. The internal logic will be junction isolated up-diffused I^2L and the interfacing will be LST^2L. At present the minimum prop delays are about 10nsec per gate for this structure. ITT has published information about advanced structures using improved doping profiles and oxide isolation.[47] These two advanced structures are shown in Figures 2.5 and 2.8, respectively. They are developing a 4K static RAM using

an advanced structure and a minimum geometry RAM cell circuit. They anticipate getting the 4K RAM on a chip 150 mil X 150 mil. The RAM development is not high priority because they do not feel they can break into the memory area in a big way.

2.4.7 National Semiconductor

The effort in I^2L at National Semiconductor has been low priority. They have three circuits under development including a watch chip and two circuits for communications systems. Their position is that for their commercial LSI products, NMOS is a better alternative.

2.4.8 Northrop

Northrop Research and Technology Center began work on I^2L in 1973 and has presented papers on the radiation response of I^2L.[24, 38] Their first work involved characterization and optimization of baseline I^2L. This work was supported by the Army Electronics Command (ECOM)[39, 40] as well as Defense Nuclear Agency (DNA). The ECOM work involved the design, construction and characterization of a frequency synthesizer as well as a study of the performance versus cost tradeoffs for optimizing baseline I^2L. The DNA work was primarily a radiation effects characterization and modeling study on baseline I^2L. Although the ECOM and DNA work was directed toward baseline I^2L, Northrop has investigated many other I^2L structures, both for radiation hardening and improved speed. Among the structures investigated were thin epitaxial "baseline" I^2L, substrate fed logic, p epitaxial I^2L, and more recently ion-implanted and Schottky base I^2L. With the use of an I^2L device physics model incorporating neutron degradation, they predict neutron hardness of greater than 10^{14} n/cm^2 on baseline I^2L MSI devices utilizing a very thin n epitaxial, optimized doping levels, and minimum geometries. Their present approach to radiation hardened I^2L is a Schottky base structure. This approach is taken to increase packing density by reducing the number of metallization runs since a single collector output can be connected to multiple inputs. In addition to the reduced metal runs, the cell size for a single collector, multiple base structure is much smaller than an equivalent function conventional structure. Northrop has several development programs under way for military applications. Among these are two circuits for inertial guidance microprocessor interfaces (a 3 X 4-bit up-down counter/MUX buffer

register and a 6 X 16-bit counter/MUX), a single chip control signal generator (binary counter, latches, ROM) for Laser Guided Projectile guidance control logic, and a 16 bit accumulator add/subtract circuit for a Fast Fourier Transform-type signal processor. The program at Northrop Research and Technology Center is directed toward support of Northrop systems divisions. Thus a major effort is the development of a custom I^2L circuit design and fabrication capability for special military systems applications. They are developing a cell library of I^2L logic functions to perform computer aided circuit design of custom circuits.

2.4.9 Hughes Semiconductor

Hughes Semiconductor has been active in developing high speed I^2L for about two years. Their approach to high performance I^2L is the use of optimized impurity profiles. A highly doped p region is deposited on an n+ substrate and an n epitaxial is grown. During the epi growth, the p region up-diffuses partially through the epi forming the base region of the npn transistor. P+ diffusions form the emitter and collector of the pnp and contacts to the npn base.[49] Isolation of the npn collectors is obtained by Schottky contacts to the n epitaxial. The npn base contacts can be either conventional or used to form a Schottky clamp between the collector and base of the npn. Both the Schottky-clamped and Schottky-contact structures increase the speed. Minimum prop delays of 2-3 nsec have been achieved with the Schottky structures. The inverted npn gains are typically 100-200 compared to 10-20 on baseline I^2L. The improvements in gain are due to the doping profile which is roughly the inverse of a "baseline" diffused profile.

Hughes is building a successive approximation register (SAR) with the up-diffused process which will be used in an A-D converter for a NASA System built by a Hughes Systems group. The SAR is ECL interfaced and has double layer metallization. Hughes is presently developing a test chip which has several MSI level building blocks used in a 4 bit slice CPU similar to the AMD 2901. They plan to market an I^2L version of the 2901 within two years.

2.4.10 Harris Semiconductor

The effort at Harris Semiconductor in I^2L has involved about 3 man years supported by IR&D funds prior to FY77. They have no product on the market and have only worked with test circuits. Their main interest is the military market in general and radiation hardened I^2L in particular. After considering possible changes to the baseline I^2L process which might improve the neutron and total dose response, Harris decided to experiment with substrate fed logic, shown in Figure 2.7, which had been announced by Plessey in 1974.[22] DNA , through NAVWPNSUPPCEN Crane, has funded a study at Harris to characterize the electrical and radiation effects performance of substrate fed logic. The present Harris program in SFL involves characterization, analysis and radiation effects testing of three MSI devices and several test structures including ring oscillators, inverters, etc. The three MSI circuits are a functional equivalent of the 54181 ALU, a 32 bit shift register and a 1K ROM. The first test devices built by Harris using the SFL approach yielded minimum prop delays of 9 nsec and npn transistor up gains of 25.[36] If the results of the present efforts are promising, Harris is planning development of a microprocessor, RAMs, ROMs, and large custom logic arrays for future product.

2.4.11 General Electric

The I^2L program at General Electric's Re-Entry and Environmental Systems Division, supported by IR&D funding, has been active for about two years. The major interest has been in optimizing baseline I^2L for performance and radiation hardening for military systems applications. The FY75 IR&D program involved modeling I^2L radiation effects (primarily neutron) in order to identify topological and process techniques which would improve inverter cell hardness.[26] This effort has identified a cell layout scheme, epitaxial thickness and doping density that have yielded four output inverter cells with neutron failure levels an order of magnitude greater than for their standard reference structure. The total dose failure level is in excess of 10^6 rad (Si). The FY76 IR&D program at G.E. is directed toward designing a Programmable Logic Array (PLA) circuit containing a large number of I^2L cells which will have a series of metallization masks to perform a variety of MSI level logic functions. These circuits will be evaluated for neutron, total dose, transient upset, and burnout radiation effects. The circuits will also be used to verify the electrical performance goals and provide data for correlation with computer model predictions.

2.3 SUMMARY OF I^2L TECHNOLOGY

The eleven companies discussed in this section represent the major commercial I^2L efforts and the major efforts to improve the radiation hardness of I^2L. However, the list is not comprehensive. I^2L work is also going on at Microcomponents, Bell Telephone Labs, Boeing, Stewart Warner Semiconductor, Westinghouse, Exar, and others. I^2L is a rapidly developing technology and is approaching maturity at several firms. However, even though several custom I^2L circuits are in production and are being used in consumer products, there are only five commercially available I^2L parts as of January 1977. A status of I^2L production and development of commercial parts is given in Table 2.2. Two of these parts, the Fairchild 9408 Microprogram Sequencer, and the T.I. SBP9900, use second generation I^2L processes. The others use either a non-isolated or junction isolated version of "baseline" I^2L. The maximum clock rate for any of the available parts is 10 MHz.

Most companies have started their I^2L work with the relatively simple "baseline" process which can easily be fabricated on a linear processing line. But while the processing is simple and reasonable performance can be demonstrated on inverter cells, ring oscillators and flip flops, there are considerable problems in going to a high density LSI device. This, of course, is true for any LSI technology, but it explains why there are very few I^2L devices presently in production even though many companies have been working on the technology for several years. The second generation, high speed forms of I^2L require further process controls and greater processing complexities which pushes their maturity further away. One of the major issues which influences the availability of commercial product is, of course, the market, i.e., where do the companies feel I^2L can compete with other technologies in cost and performance. Because of processing, cost and performance considerations I^2L development has proceeded in the following ways:

1. Analog/digital devices using isolated "baseline" I^2L

Because I^2L can be combined with linear circuits on the same chip there is a wide range of applications for reducing the number of packages to perform functions requiring both digital and linear devices. There is a large market for single chip controllers in such products as watches, cameras, appliances, automotive and TV. Another large market is instrumentation such as digital

TABLE 2.2
STATUS OF COMMERCIAL I^2L

VENDOR	PARTS IN PRODUCTION (*DENOTES COMMERCIALLY AVAILABLE)	PARTS IN PILOT PRODUCTION OR DEVELOPMENT
Texas Instruments	*SBP0400 - 4 bit parallel Binary processor element *AC5902Y - Five function LED watch circuit *SPB9900 - 16 bit microprocessor	SN54S400 - 4096 bit static RAM Custom Circuits for camera Keyboard encoder T.V.
Fairchild	*9408 - Microprogram Sequencer 93481 - 4K dynamic RAM	9412 CRT controller 9423 FIFO 9440 CPU
Signetics	*8X01 Cyclic Redundancy Character Generator/checker *8X04 FIFO	6 Function Watch Chip 64 X 8 FIFO 16 X 8 LIFO Long Timer Circuit Code/Decode Circuit
Motorola	Divider Circuit (Organ)	8-10 Analog/Digital for Controllers and Communications
RCA	Panel Meter Chip	Analog Watch Chip 7 Function Watch Chip
ITT	6 Devices, All Watch and Watch/Calculator Interface	3-4 MSI/LSI LST^2L Replacements
Hughes	-	Successive Approximation Register 2901 Bit Slice
National	-	Watch Chips

panel meters where I^2L has already been applied. Although optimum I^2L performance is achieved with low voltage amplifiers, reasonable I^2L performance can be achieved with 20 or 30 volt amplifiers. Thus I^2L will probably find a large market in A/D and D/A converters.

2. Digital LSI Arrays

Both isolated and non-isolated "baseline" I^2L have been applied to the digital LSI market. However, because of the speed limitations of the baseline process the major impact on the digital market will be with second generation forms of I^2L. Standard functions such as CPU, memory, computational and control functions will require the higher speeds available with second generation I^2L. There may be a custom circuit market for "baseline" I^2L utilizing gate configurable arrays or full custom design if the speed requirements on the custom circuits are modest. But the major market for digital LSI I^2L will probably be with the higher speed structures.

Because of these considerations it is difficult to define "commercial" I^2L. In order to improve the performance of I^2L for computer applications the following variations have been employed:

1. For Speed.
   a. Schottky clamps and contacts.
   b. Ion implantations.
   c. Thinner epitaxial layers.
   d. Oxide isolation (V-groove, anodic, Isoplanar)
   e. Up-diffusion.
2. For Packing Density.
   a. Substrate injector.
   b. Dual level metallization.
   c. Oxide isolation.
   d. Multiple Schottky base inputs.
3. For Power Dissipation.
   a. Substrate injectors.
   b. Double diffused injectors.
   c. Buried injectors.

Although no two companies are taking the same approach to high speed I^2L some common features will probably emerge in high density, high speed products.

Some form of oxide sidewall isolation is common to most approaches. To achieve high densities, dual level metallization will be needed. Because a factor of two improvement in speed can be achieved using Schottky contacts, they probably will see rather wide use. It is difficult to say at this point in time whether the high speed commercial inverter cell structure will be up-diffused, ion-implanted, or substrate fed, but regardless of what form dominates the mature technology, it is clear that I^2L is a viable technology for future LSI.

SECTION 3

RADIATION EFFECTS CHARACTERIZATION OF I^2L TECHNOLOGY

Early papers[23,24] on radiation effects characterization of "baseline" I^2L test structures indicated severe neutron degradation, especially at low injector currents. While these results would indicate a very limited use of I^2L for radiation hardened applications, many people in the radiation effects community felt that the second generation form of I^2L designed primarily to increase speed, would result in increased neutron hardness. Although not all forms of second generation I^2L have been characterized for radiation effects, those forms which have been tested verify the expected increase in neutron hardness.

In this section the radiation induced failure mechanisms for neutron, long-term ionization and dose rate environments are analyzed and radiation data taken on "baseline" and several second generation I^2L structures is presented. Data taken by NAVWPNSUPPCEN Crane is discussed in detail and data taken by other agencies is summarized.

3.1 NEUTRON EFFECTS

Neutron effects characterization analysis and test results are given first on "baseline" I^2L structures and then on various forms of second generation I^2L.

3.1.1 Evaluation of Neutron Effects In First Generation I^2L

Because I^2L is a bipolar technology the basic neutron failure mechanisms for I^2L are the same as for other bipolar devices. Neutrons cause bulk displacement damage which increases the number of recombination and trapping centers. An increase in the number of recombination centers decreases minority carrier lifetime, and an increase in the number of trapping centers increases resistivity. For baseline I^2L, the changes in resistivity can be ignored at neutron fluences of interest since the carrier removal rate is on the order of 2-3 carriers per unit neutron fluence and doping levels are in excess of $5 \times 10^{15}/cm^3$. Therefore, only changes in lifetime need be considered for this analysis. The discussion pertaining to the effects of minority carrier lifetime changes on the operation of an I^2L inverter cell will be based on the assumption of a constant injector current. An illustration of the baseline I^2L structure with the major current components is shown in Figure 3.1.

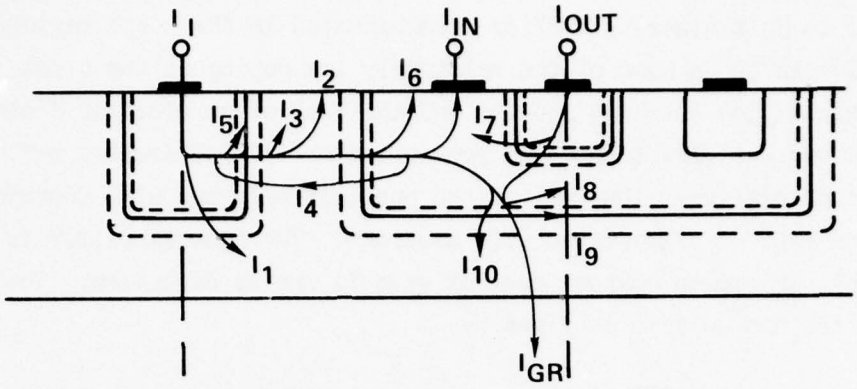


Figure 3.1 Major Components of Current In An I^2L Inverter

The injector current (I_I) is injected across the entire injector to n epi junction. That portion of I_I which crosses the n epi to CP junction is available to satisfy recombination in the npn base region. This fraction, represented by the common base current gain of the lateral pnp transistor (α), is typically measured by grounding the substrate, injecting current into the injector and measuring the fraction of current collected at the input with the input grounded. α is given by the expression

$$\alpha = \frac{I_{IN}}{I_I} \sim 1 - \frac{(I_1 + I_2 + I_3 + I_4 + I_5)}{I_I}$$

The five significant components of lateral pnp base current which degrade the value of α from its optimum value of one are :

1. I_1 - Current injected downward toward the substrate which recombines in the n epi or n+ substrate.
2. I_2 - surface recombination current both in the neutral base and space charge regions.
3. I_3 - Bulk neutral base recombination current.
4. I_4 - Current back injected from the pnp collector toward the injector.
5. I_5 - Emitter-base space charge recombination current.

Neutron irradiation increases primarily components I_1, I_3 and I_5 because of the increase in bulk minority carrier recombination in the n epi region. This affects α significantly because of the relatively low doping of the n epi, the width of the base region (usually 4-6 μm) and the lack of an electric field in the base to aid current flow toward the pnp collector. These factors not only contribute to the relatively low gain of the pnp initially but also contribute to the increased rate of degradation with neutrons. The npn transistor is characterized by the common emitter current gain in the up direction. The expression for the npn up gain is given by

$$\beta_u = \frac{I_{OUT}}{I_{IN}} \simeq \frac{I_{OUT}}{I_4 + I_6 + I_7 + I_8 + I_9 + I_{10}}$$

where

1. I_6 - Neutral base and depletion layer surface electron recombination current.
2. I_7 - Neutral base electron recombination current in the extrinsic base region.
3. I_8 - Neutral base electron recombination current in the extrinsic base region.
4. I_9 - Emitter-base space charge electron recombination current.
5. I_{10} - Hole current back injected toward the emitter(n epi).

The two major components[58] of npn base current before neutron irradiation are the hole currents back injected toward the emitter (I_4 and I_{10}) and the extrinsic base recombination (I_7). These terms are representive of the emitter efficiency and collector efficiency respectively. The emitter efficiency is low in this structure because of the relatively low ratio of the doping levels on either side of the emitter-base junction and because the emitter region has no electric field to oppose hole flow from the base region. The collector efficiency is low because of the low ratio of collector area to emitter area.

After neutron irradiation minority carrier recombination increases result in an increase in I_7, I_8, and I_9 as well as the emitter efficiency. The increase in I_8 is greatly enhanced because of the electric field in the intrinsic base region which opposes electron flow. The value of I_9 increases rapidly with neutron irradiation because the recombination rate in the space charge region is much greater than in the bulk and this structure has a relatively large emitter-base space charge region.

Because of the nature of the merged I^2L structure the cell fanout degrades rapidly with neutron irradiation for a constant value of injector current due to both pnp α and npn β_u degradation. Since the injector efficiency degrades with neutrons, the minimum operating current level of the cell increases. This degrades cell fanout, since the degradation of β_u is also greater at lower current levels. The current dependence of the β_u degradation is primarily due to the degradation of the space charge recombination term (I_9) which has a reciprocal slope value of ~ 1.5, i.e., $I_9 \simeq I_R \exp \frac{qVBE}{1.5kT}$.

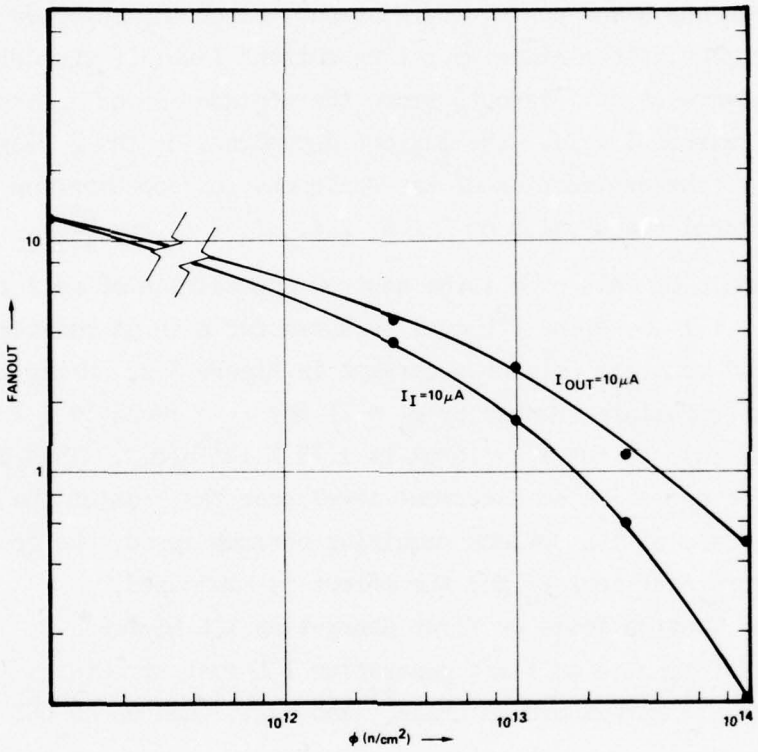
As an example of this effect the neutron degradation of cell fanout for a single collector T.I. baseline I^2L cell is shown for a 10 μA constant injector current and a 10 μA constant collector current in Figure 3.2. Using this data, the fluence of failure (Fanout or β_u = 1) for I_C = 10 μA is 4 X 10^{13}n/cm^2 and the fluence of failure for I_I = 10 μA is 1.75 X 10^{13}n/cm^2. This effect is greatly reduced for operation at a current level near the peak of the β_u vs. I_C curve. In the case of I^2L devices requiring optimum speed, the operating point usually occurs near peak β_u and the effect is minimized.

3.1.2 Results of Neutron Tests on First Generation I^2L Devices

Neutron test results on first generation I^2L test structures have been reported by Northrop,[24] NAVWPNSUPPCEN Crane,[23] and G.E.,[28] and on an LSI circuit by Boeing.[41]

The Northrop tests were performed on single and three output inverter cells and five stage ring oscillators fabricated in their own laboratory. The fanout per collector (approximately equal to β_u) degraded to a value of one at ~ 4 X 10^{13} n/cm^2 for operation at 1 μA output current and 7-8 X 10^{13} n/cm^2 at 100 μA. This data is probably representative of the best case single output inverter. At 3.5 X 10^{13} n/cm^2 four of the eight ring oscillators failed to operate.

The NAVWPNSUPPCEN Crane data was taken on test structures built by Texas Instruments. This data was also taken on single collector inverters and five stage ring oscillators.



Fanout vs Neutron Fluence for a Single Collector
First Generation I^2L Inverter Cell

Figure 3.2

The failure levels for the inverter cell ranged from ~ 1.5 X 10^{13} n/cm^2 at I_C = 1 μA to ~ 6 X 10^{13} n/cm^2 at I_C = 100 μA. The ring oscillators failed to operate at ~ 3 X 10^{13} n/cm^2.

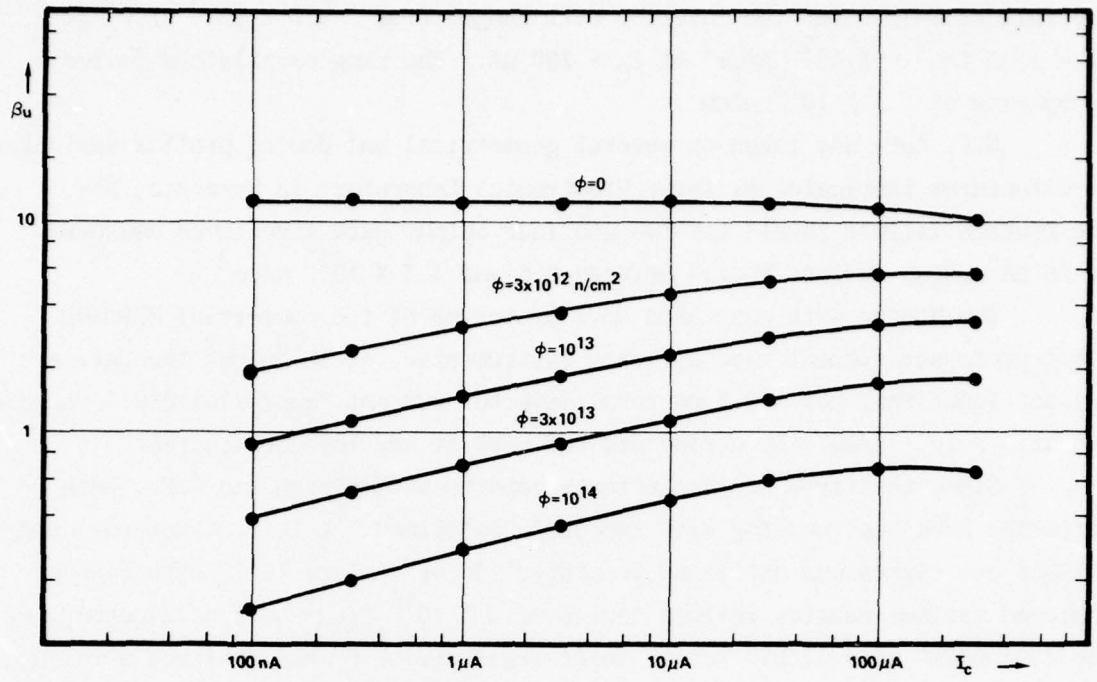
G.E. data was taken on several geometrical and doping profile variations of structures fabricated by their Electronics Laboratory in Syracuse, N.Y. The neutron failure levels for two and four output gate structures measured at 50 μA output current varied between 0.6 and 3.3 X 10^{13} n/cm^2.

The Boeing data was taken on a prototype of the commercial SBP0400 4 bit processor element made by Texas Instruments. At 10^{13}n/cm^2 the device was not functional below 5.6 mA total injector current (approximately 4 μA/gate) and at 4 X 10^{13} n/cm^2 the device did not work at any injector current.

Since the first neutron effects reports by Northrop and G.E., both companies have been working with improved "baseline" I^2L test structures using thinner epi layers and optimized geometry. As of January 1977 Northrop has achieved maximum neutron failure levels of 2 X 10^{14} n/cm^2 on single output cells and 10^{14} n/cm^2 on a 32 bit serial shift register. G.E. has achieved a failure level of 7-8 X 10^{13} n/cm^2 on four output inverter cells. Work is still going on by both of these companies to extend the neutron hardness of the "baseline" I^2L process.

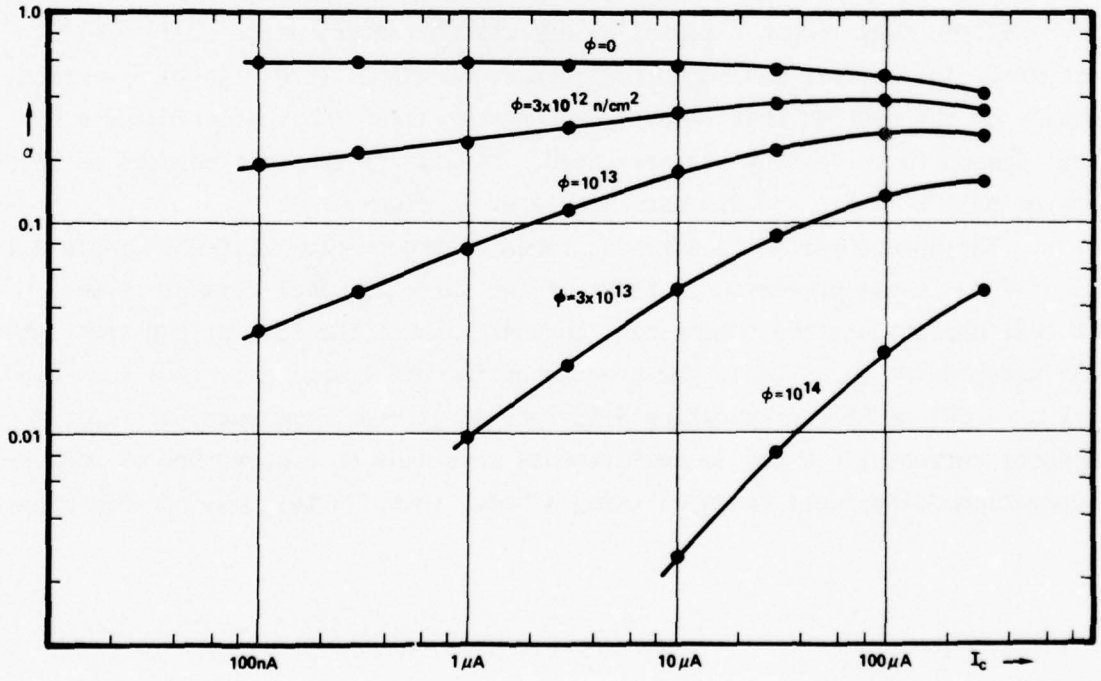
In 1974 NAVWPNSUPPCEN Crane, supported by the Strategic System Project Office of the Navy, began a radiation effects characterization study on I^2L circuits. This effort was supported in part by DNA in 1976. In this section, details of the neutron test results on the "baseline" I^2L test structures investigated in this study are presented. Details of the test results on second generation I^2L sample are discussed in later sections.

The data compiled to date was taken on the samples listed in Table 3.1. All of the data is presented in terms of the three critical parameters for I^2L cell operation: the common base current gain of the lateral pnp transistor (α) (measured at V_{CB} = 0V.), the up gain of the npn transistors (βu) (measured at V_{CB} = .5V) and the propagation delay per stage (tpd) (measured at various injector currents). α and βu measurements were made on a curve tracer and the propagation delays were measured using a bench test. A test was performed on



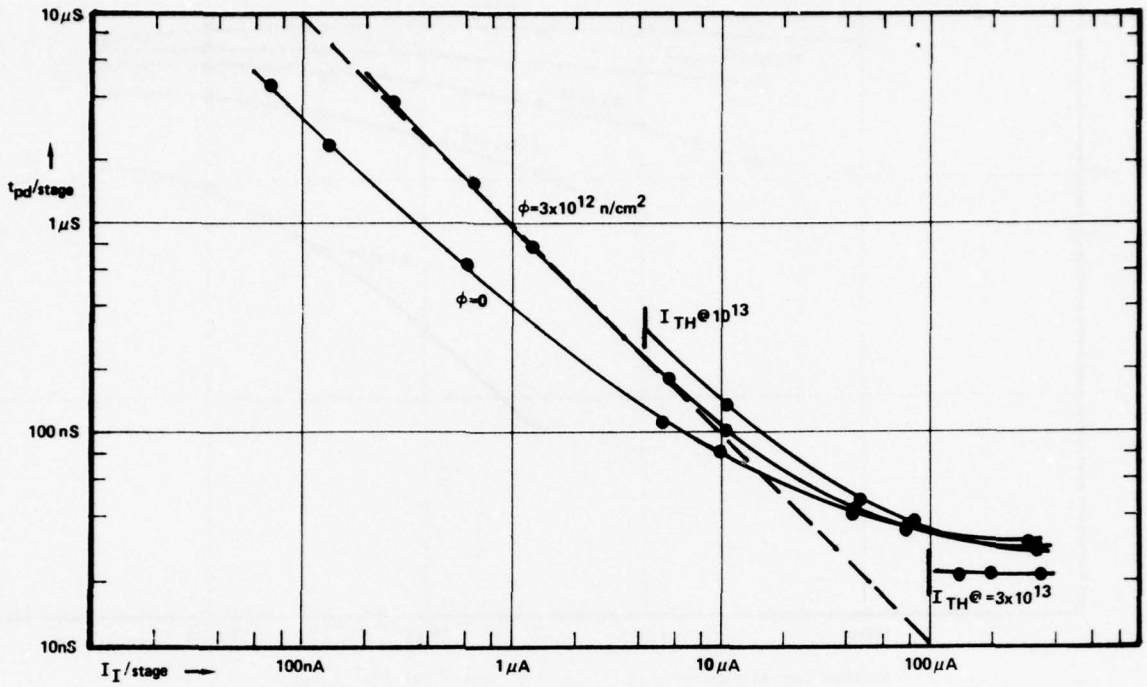
Neutron Degradation of βu vs I_C for T.I. First Generation I^2L Development Chip

Figure 3.3



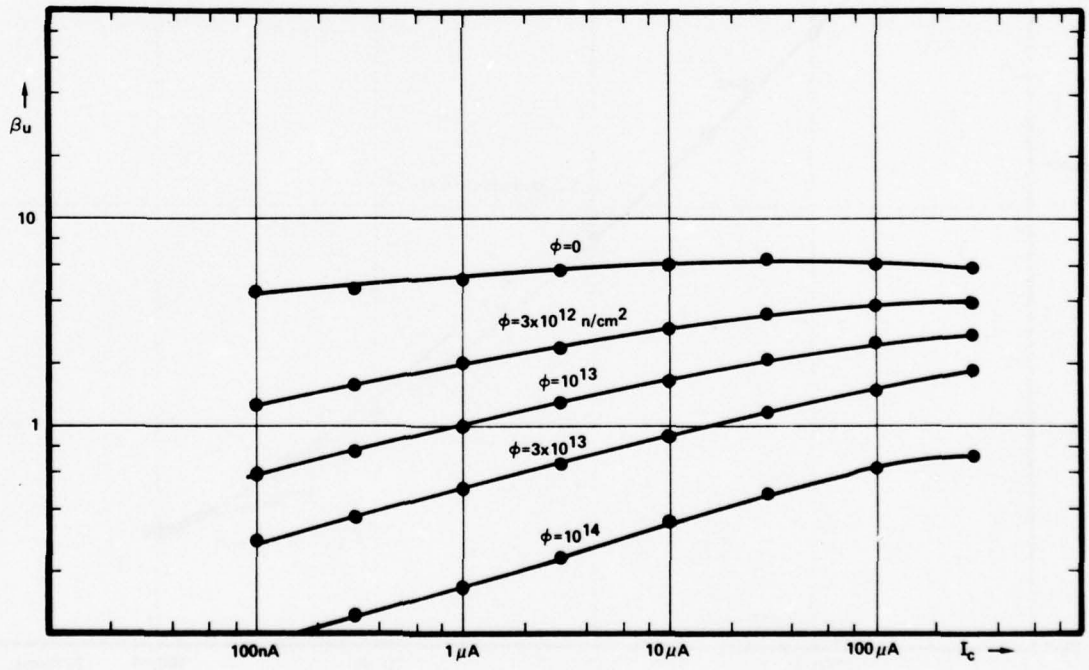
Neutron Degradation of α vs I_I for T.I. First Generation I^2L Development Chip

Figure 3.4



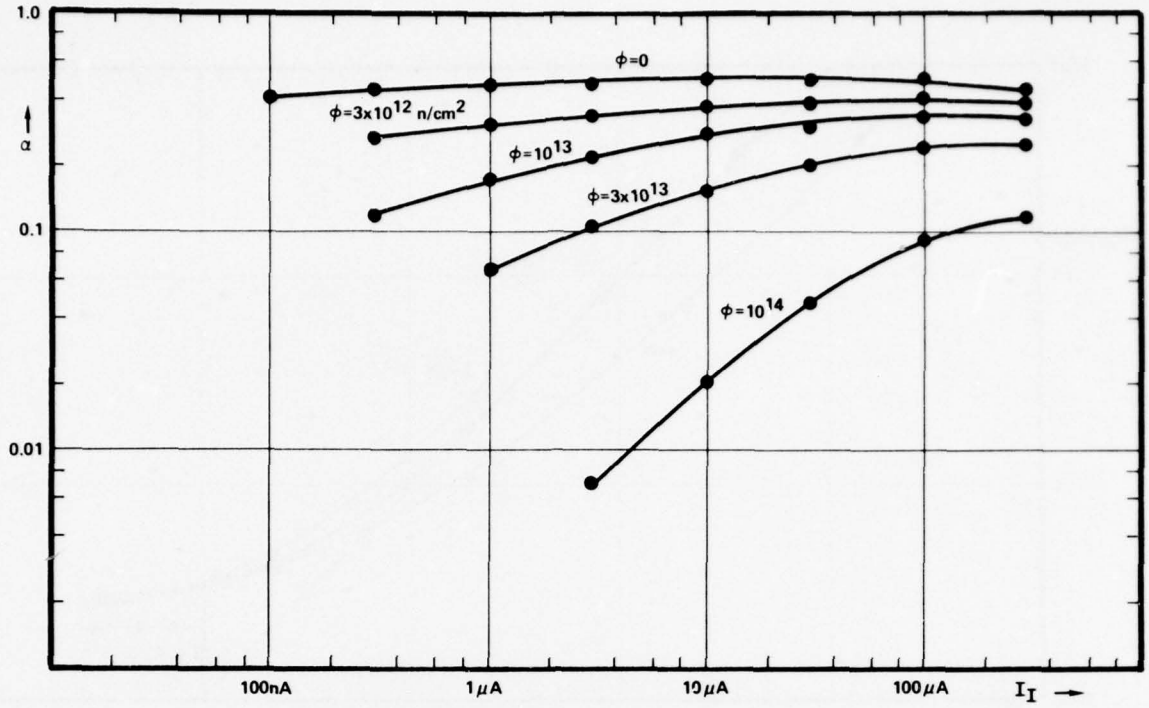
Neutron Degradation of tpd Per Stage vs I_I Per Stage For The T.I. First Generation I^2L Development Chip

Figure 3.5



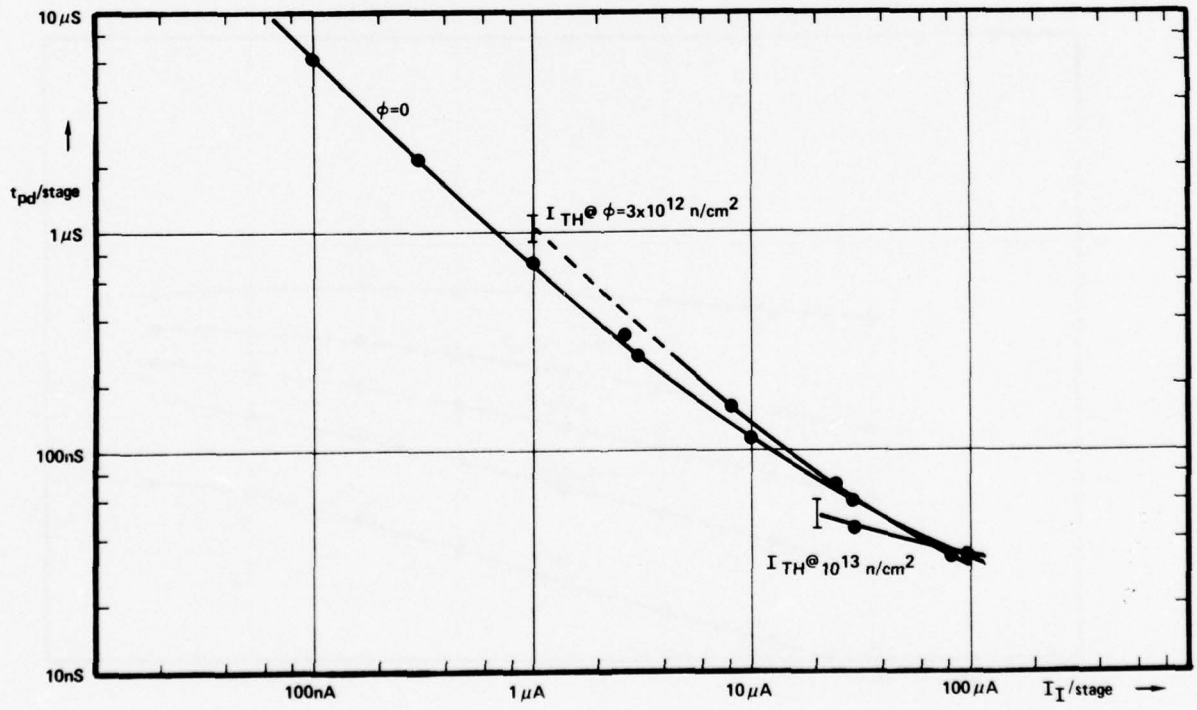
Neutron Degradation of βu vs I_C for T.I. X0400 Test Structures

Figure 3.6



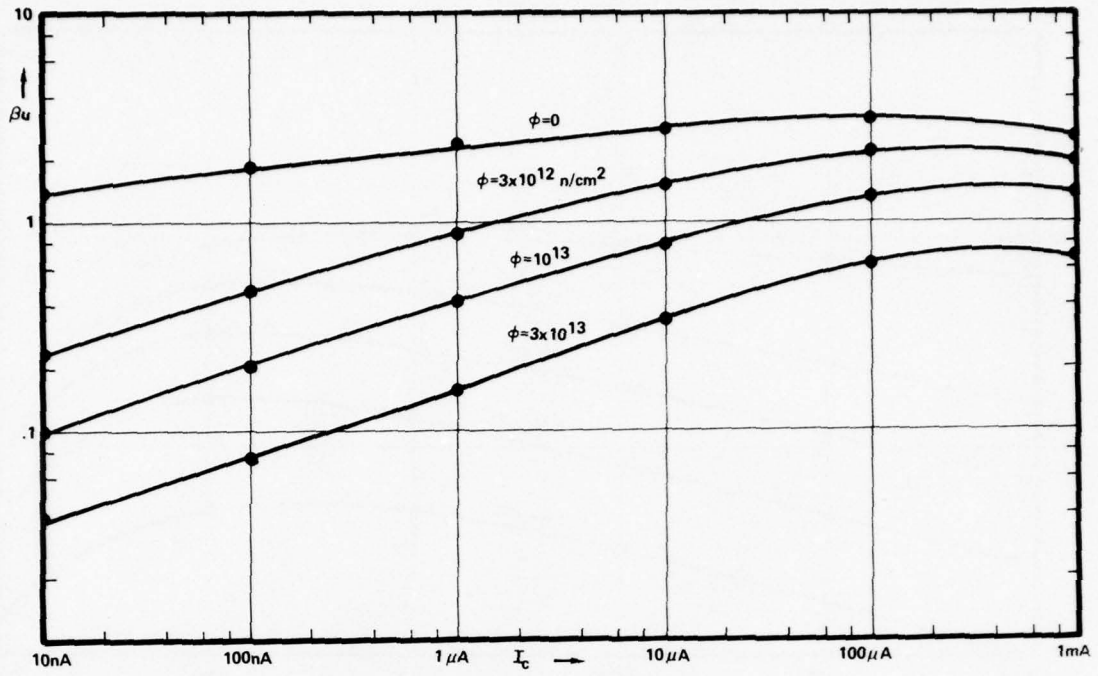
Neutron Degradation of α vs I_I for T.I. X0400 Test Structures

Figure 3.7



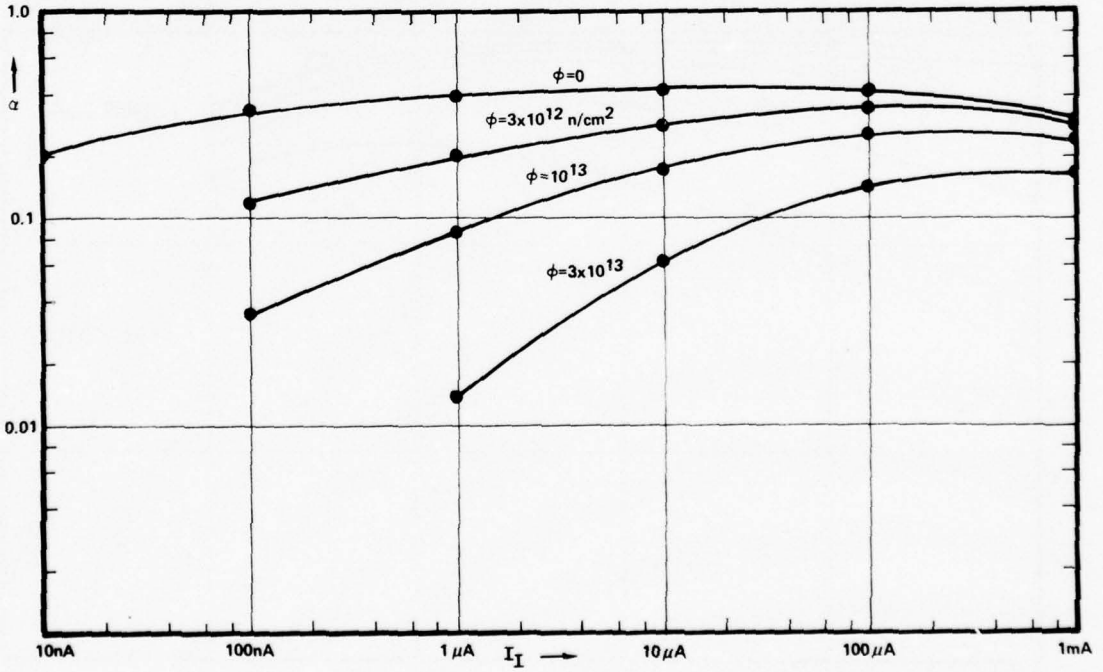
Neutron Degradation of tpd Per Stage vs I_I Per Stage for T.I. X0400 Test Structures

Figure 3.8



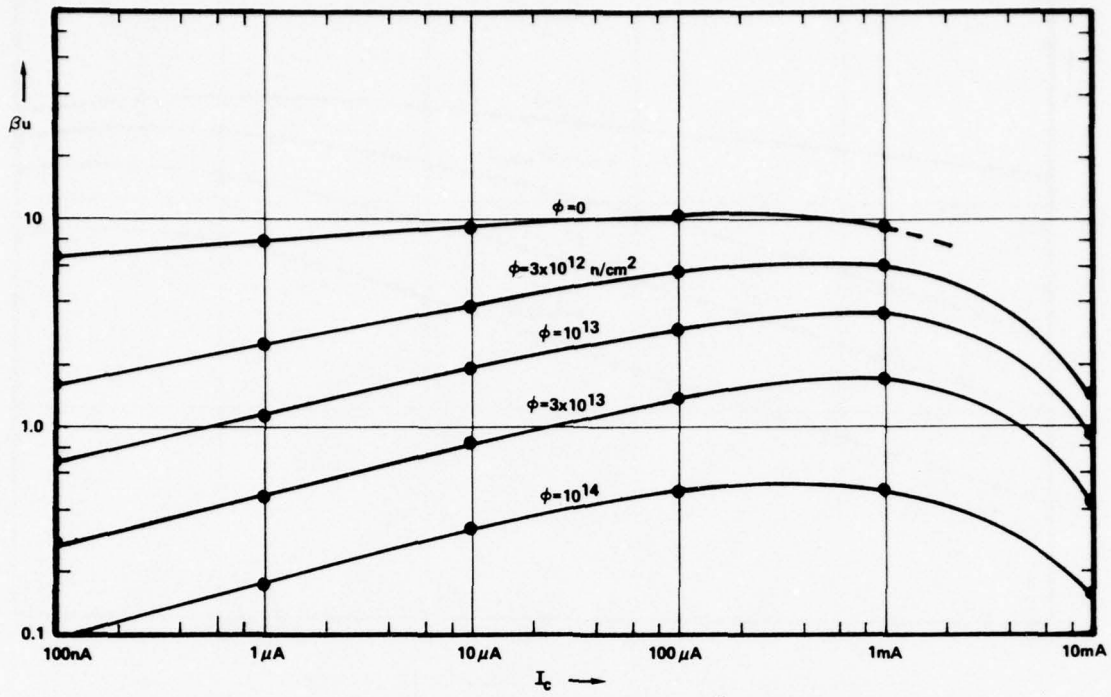
Neutron Degradation of βu vs I_c for RCA First Generation I^2L Development Chip

Figure 3.9



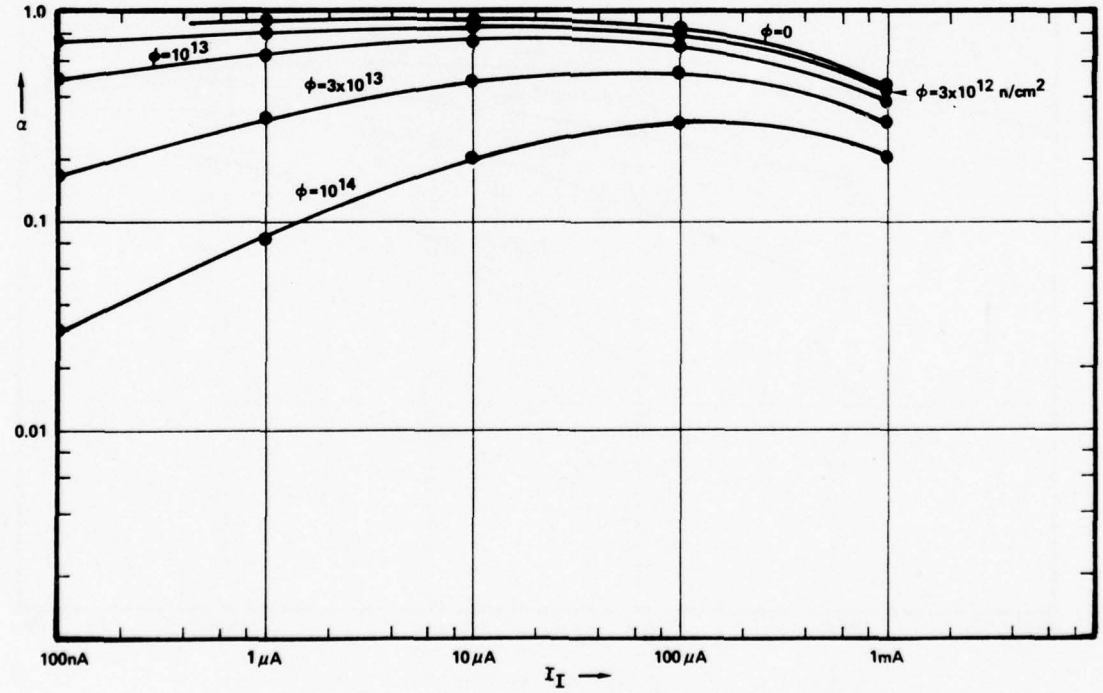
Neutron Degradation of α vs I_I for RCA First Generation I^2L Development Chip

Figure 3.10



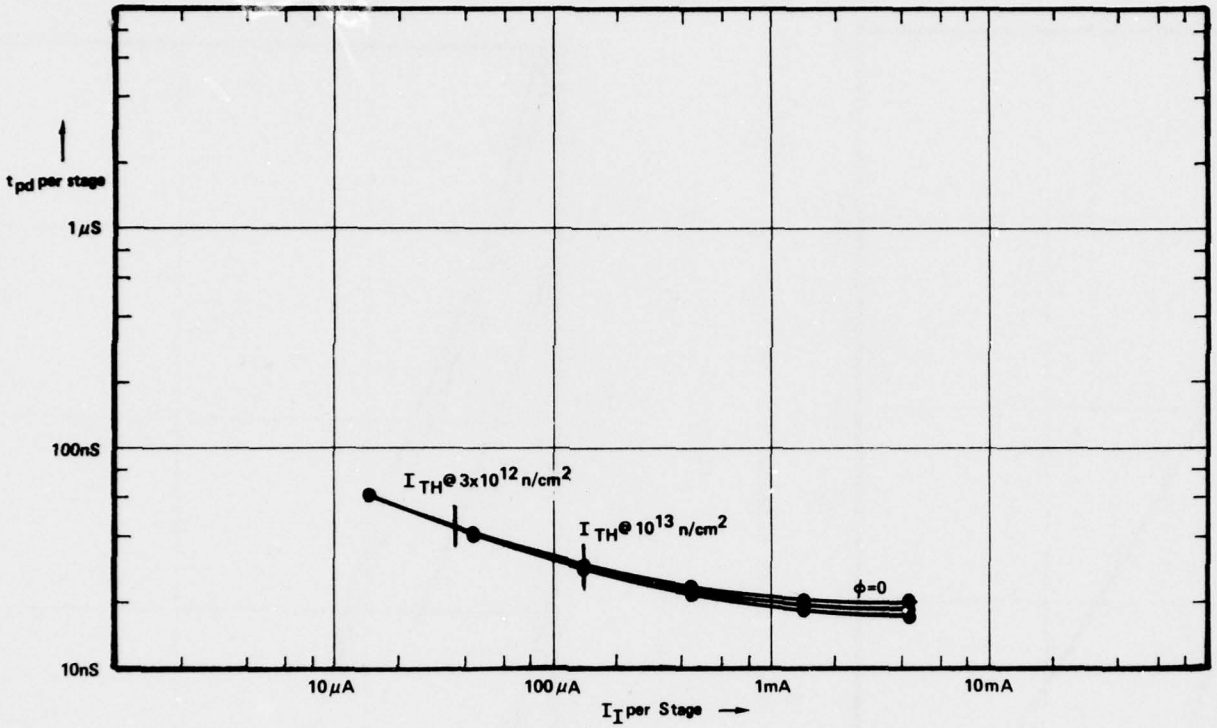
Neutron Degradation of βu vs I_C for Harris First Generation I^2L Development Chip

Figure 3.11



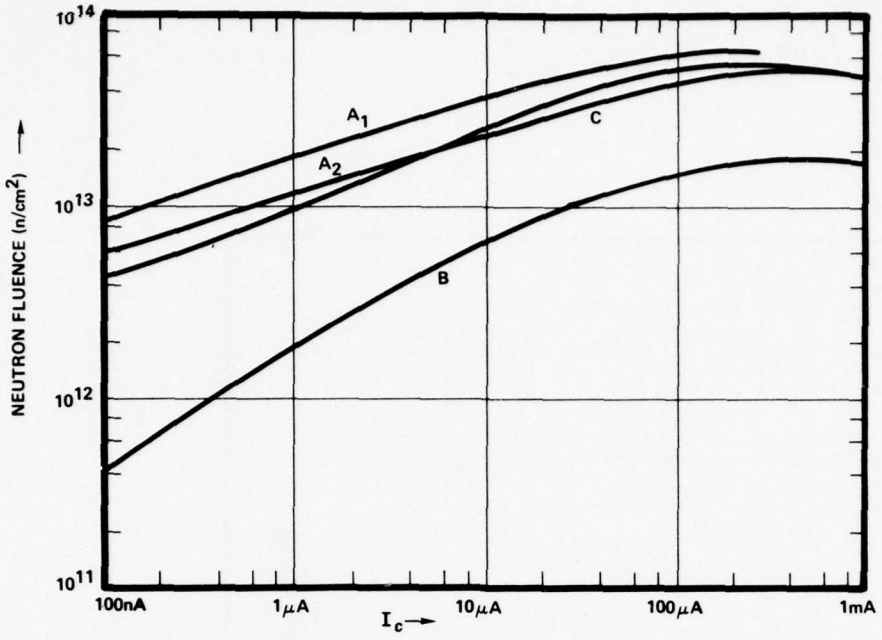
Neutron Degradation of α vs I_I for Harris First Generation I^2L Development Chip

Figure 3.12



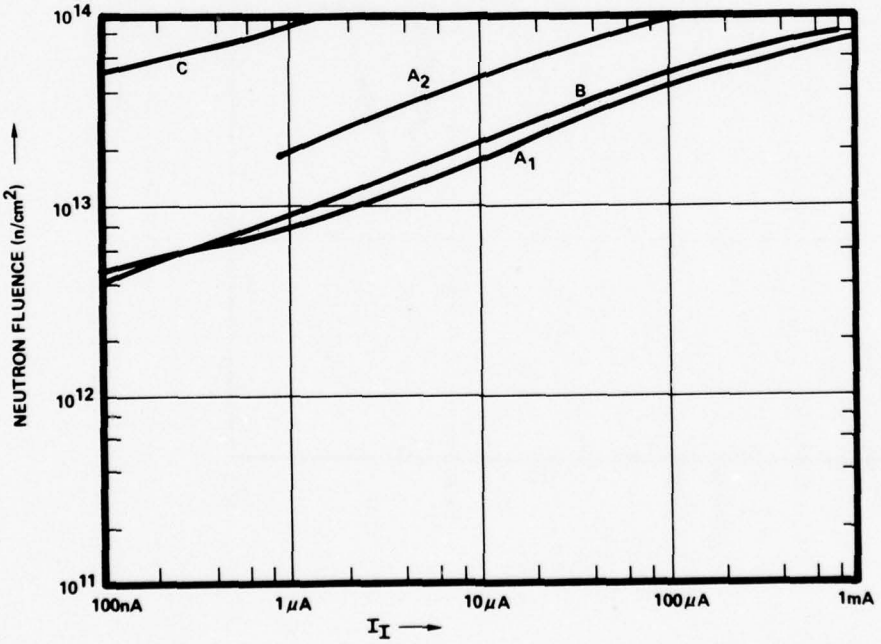
Neutron Degradation of tpd Per Stage vs I_I Per Stage For Harris First Generation I^2L Development Chip

Figure 3.13



Neutron Fluence Required to Degrade βu to One vs I_C in First Generation I^2L

Figure 3.14



Neutron Fluence Required to Degrade α to 0.1 vs I_I in First Generation I^2L

Figure 3.15

each inverter cell type to assure that βu measurements were representative of actual circuit fanout. The worst case difference observed for single collector cell up to 100 μA was ~5% with βu having the higher value. For multiple collector cells operated at currents >100 μA, β_{eff} may be significantly lower than βu and caution must be used in projecting radiation failure levels from βu measurements. α measurements are plotted vs. injection current before irradiation and at the various test fluences, βu is plotted vs. collector or output current, and prop delay per gate is plotted vs. injector current per gate.

Table 3.1 List of First Generation I^2L Test Structures Evaluated By Crane

Code	Vendor	Description of test chip and structures available at external pins	Number of Samples used for Neutron Tests
A_1	T.I.	Development chip - one 5 stage ring oscillator, two single collector inverters.	5
A_2	T.I.	Structures on SBP0400 - two 5 stage ring oscillators and one 3 collector cell.	1
B	RCA	Development chip - two 3 collector cells, one 5 collector cell	2
C	Harris	Development chip - (n substrate) one 7 stage ring oscillator one single collector cell.	3

All of the irradiations were performed on the White Sands Missile Range Fast Burst Reactor. Graphs of the three parameters for each of the structures are presented in Figures 3.3 through 3.13. All data points are average values. There are no prop delay graphs for RCA devices due to the absence of ring oscillator test structures.

A summary of the neutron effects test results on the seven sets of samples is given in Figures 3.14 and 3.15. Chosen for comparison is the neutron fluence required to degrade βu to a value of one as a function of output current (Figure 3.14) and the neutron fluence required to degrade α to a value of 0.1 as a function of injector current (Figure 3.15). The code letters refer to the manufacturer as indicated in Table 3.1. The data is presented to illustrate the strong dependence of neutron degradation of the operating current and wide variation in neutron hardness between various "baseline" I^2L processes.

3.1.3 Analysis of Neutron Effects in Second Generation I^2L

The neutron hardness of baseline I^2L is low primarily for the same reasons that the initial current gains of the lateral pnp and inverted npn are low. In general, the changes employed in second generation I^2L to increase the transistor gains and inverter cell speed will also improve the neutron hardness. As pointed out in Section 3.1.1, the neutron hardness of first generation I^2L is affected by:

1. The wide, constant doped base of the pnp.
2. The poor emitter efficiency of the npn.
3. The large relatively low doped extrinsic npn base region.
4. The opposing electric field in the intrinsic npn base.

The second generation I^2L structures compensate for some of these deficiencies. The structures which will be discussed in this section are ion-implanted, up-diffused, substrate fed and p-epitaxial.

A discussion of ion-implanted structures was given in Section 2.3.3. The basic differences between this structure and the "baseline" structure are the use of a thinner epi, lower doped modified profile in the intrinsic npn base region, high doped extrinsic base region, and higher doped injector. The degradation of α in the pnp transistor is due primarily to hole recombination in the epi base as in the "baseline" structure. However, in this structure a narrower base region is used and the volume of epi below the injector is reduced. This reduction in total base volume reduces neutron induced recombination. Out-diffusion of the n+ substrate into the narrow epi region below the injector creates an electric field which opposes hole injection into the substrate. This increases the initial value of α which will also improve the neutron tolerance. The βu of the npn transistor is improved by eliminating the intrinsic base retarding electric field and creating a higher excess carrier concentration in the intrinsic base relative to the higher doped extrinsic base. This will help concentrate current flow in the region under the collector and minimize recombination in the extrinsic base region. The emitter efficiency term is increased by the retarding electric field in the emitter resulting from substrate out-diffusion. With these improvements, the neutron degradation of the npn transistor will be due primarily to neutron induced electron recombination in the emitter-base space charge and intrinsic neutral base regions, and increases in the lateral hole injection from the npn base toward the injector from neutron induced recombination in the epi.

Variations of the up-diffused structure are discussed in section 2.3.4. An analysis of the Hughes structure, Figure 2.6, will be given since it appears to offer better speed as well as neutron hardness. The lateral pnp structure in up-diffused I^2L is similar to that of "baseline" and ion-implanted I^2L. The major difference in the lateral pnp is that the p regions extend to the epi, the lower portion consisting of the up-diffused boron implant. By extending the injector region to the substrate, hole injection is concentrated laterally toward the pnp collector. Also, the total volume of n epi which contributes to neutron induced increases in minority carrier recombination is reduced. Typical epi thickness for these structures is 1.5 μm. The neutron degradation of the npn transistor βu should be similar to that of a conventional down diffused transistor β. The inverted profile of this structure has a highly doped emitter (substrate), a narrow graded base profile with an aiding electric field, and an epi collector. As with the ion-implanted structure, the extrinsic base regions are heavily doped. Neutron induced βu degradation will be due primarily to increased recombination in the emitter-base space charge region and increased lateral hole injection toward the injector.

Substrate Fed Logic (SFL), as fabricated by Harris, was shown in Figure 2.7. In this structure the lateral pnp is replaced by a verticle pnp with the substrate injecting current uniformily across the chip. This vertical pnp has a highly doped emitter, a relatively highly doped uniform base and a lower doped collector. This will give high injection efficiency, especially if a relatively thin n-epi base is used. For the Harris structure the n-epi thickness is 2-3 μm, compared to 4-6 μm typical of lateral pnp base widths. Neutron degradation of the SFL pnp will be due primarily to increased recombination in the emitter-base space charge region and neutral base region. This will be confined to the regions under the inverter cell because of the deep n+ diffusions which make contact to the n epi ground plane except where a cell is formed.

The npn transistor consists of an n-epi emitter, a p-epi base and an n+ diffused collector. The emitter efficiency of this structure is increased over that of the "baseline" structure since the ratio of doping between the emitter and base regions is fairly high (~20 in the present Harris structures). Lateral hole injection toward the injector is eliminated because of the vertical structure. The primary components of neutron induced base current will therefore be the increased recombination in the emitter-base space charge region (which extends across the entire cell) and increased recombination in the intrinsic and extrinsic base regions.

The form of p-epi I^2L which is most widely discussed for high speed I^2L is shown in Figure 2.9. In this structure the lateral pnp injector is double diffused to give a highly doped emitter, narrow graded base region and relatively low doped collector (p-epi). With this approach, a doping profile similar to a conventional down-diffused vertical pnp profile is achieved. The large volume low doped uniform base region which results in appreciable neutron degradation of α is eliminated. Since the base of the double diffused structure is not only narrower but has an aiding electric field, the neutron degradation will be due primarily to increased recombination in the emitter-base space charge region. The npn transistor doping profile is nearly the same as for SFL. The major difference is that the emitter (substrate) doping is higher. This should further increase the emitter efficiency over that of SFL, but the major components of neutron induced gain degradation will be the same. Although lateral hole injection toward the emitter is not eliminated, as in SFL, it is greatly reduced because of the pnp profile.

3.1.4 Results of Neutron Tests on Second Generation I^2L Test Structures

The radiation effects characterization study on I^2L at NAVWPNSUPPCEN Crane has so far included three forms of second generation I^2L. Neutron effects data has been completed on samples from the first diffusion run of Harris SFL, early runs of double Schottky up-diffused I^2L from Hughes, and "advanced" (ion-implanted) I^2L from T.I. representative of the SBP9900 process. Still in test are second run Harris SFL and ion-implanted structures from RCA.

The neutron irradiation data taken by NAVWPNSUPPCEN Crane on the first runs of Harris SFL has been published by Harris.[36] The test structures were fabricated using a mask set designed for "baseline" I^2L. No provision was made to measure the injector efficiency for a single I^2L cell, thus it was difficult to derive an actual figure for the power dissipation per gate. The published power-delay products were based on a ratio of active cell area to total chip area. The samples tested by Crane had one single collector inverter cell, one individual npn transistor, and a seven stage ring oscillator bonded out.

A total of twelve samples were irradiated on the White Sands FBR. Three samples were irradiated at $10^{13}n/cm^2$, three at $3 \times 10^{13}n/cm^2$, three at $10^{14}n/cm^2$ and three at $3 \times 10^{14}n/cm^2$. Measurements were taken on βu, β_{down} (reversing collector and emitter), α_{down} and prop delay. α_{down}, the fraction of current

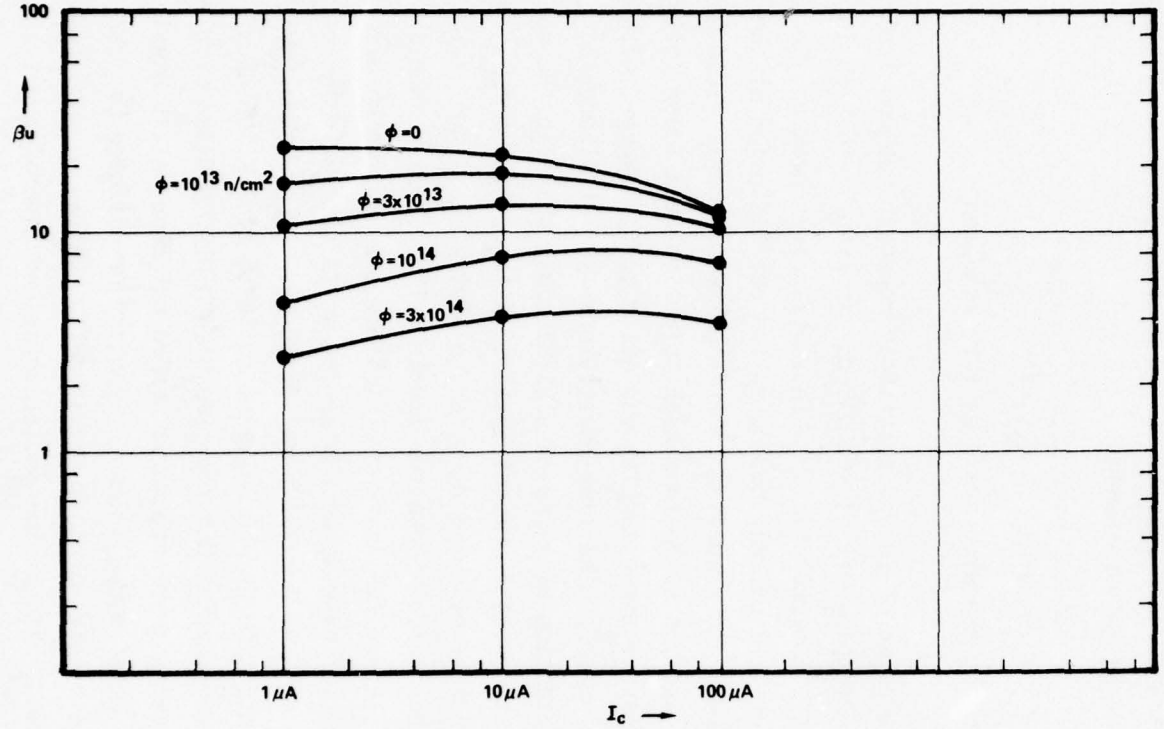
injected from the p-epi and collected at the substrate, was measured since the normal α measurement in non-isolated SFL is not meaningful. The BV_{CEO} of the npn transistors was quite low (0.5-1.5V), therefore βu measurements were made at a V_{CE} of 0.2V. A plot of βu vs I_C is shown in figure 3.16 and propagation delay (t_{pd}) vs total injector current is shown in figure 3.17. The preirradiation βu value at each current is the average of all 12 samples. The degraded βu values were calculated from the average damage coefficient for each irradiated group using the expression.

$$\frac{1}{\beta_{\phi}(ave)} - \frac{1}{\beta_{o}(ave)} = K\phi$$

The t_{pd} values are the measured averages for each group.

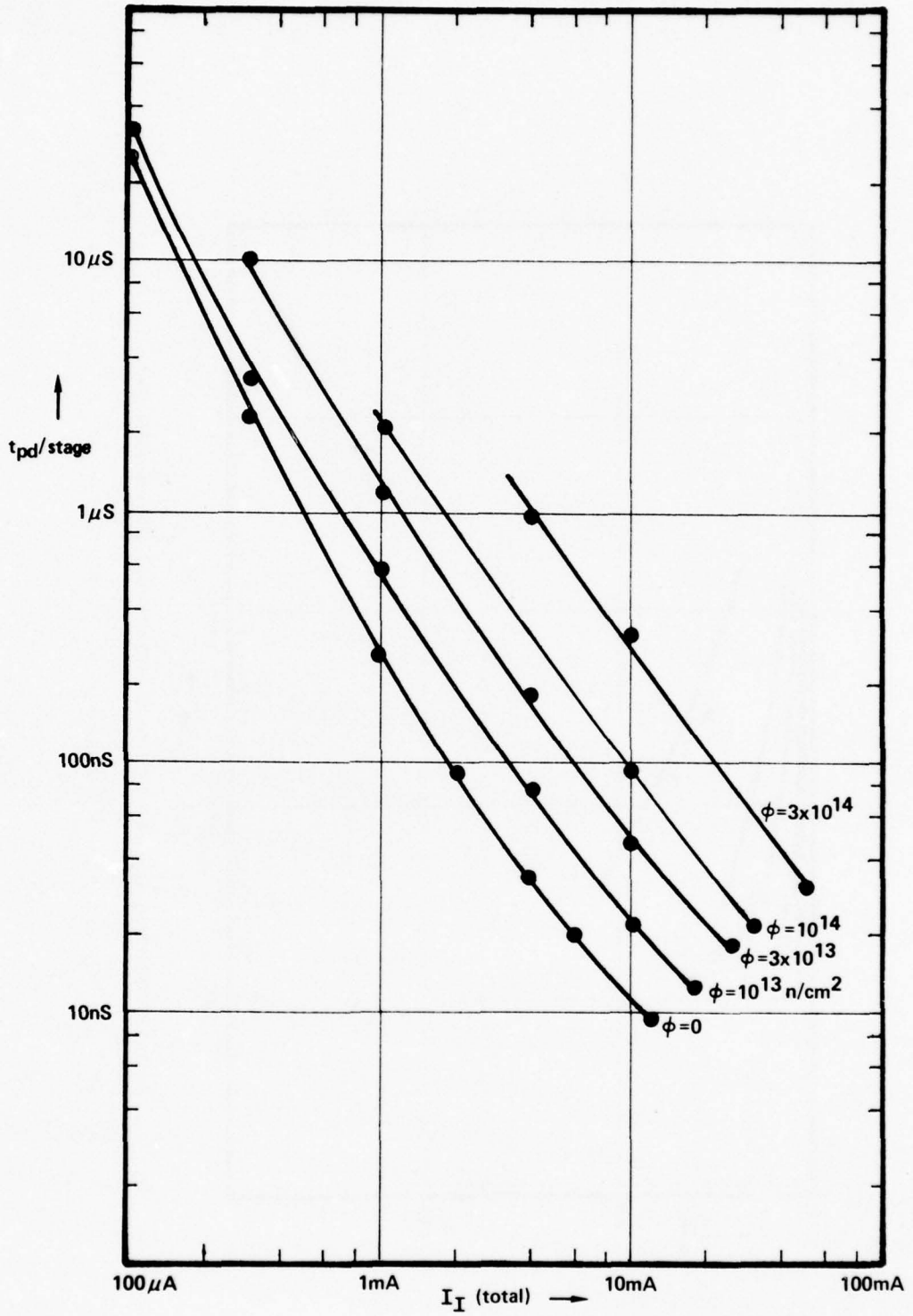
The preirradiation value of βu was relatively constant between 1 μA and 10 μA but started dropping off at 100 μA, due apparently to high injection effects. For most I^2L structures this fall off occurs between 100 μA and 1 mA. This earlier fall off may be due to the out-diffusion of the nepi impurities into the p epi base. The resulting retarding base electric field would cause the emitter-base junction to go into high injection at a lower collector current. The neutron hardness of these samples was quite good, however, with the 10 μA $\beta u = 5$ at 3×10^{14} n/cm^2. The ring oscillators were still working at 3×10^{14} n/cm^2 but the degradation of α caused a significant shift in the speed-power curve toward higher injector current levels. Although the normal injector efficiency could not be measured directly, a plot of α_{down} vs. I_{IN} is shown in Figure 3.18 for the different neutron levels. The normal α should be as good or better as α_{down} since the emitter efficiency term in the up direction is better and the emitter base space charge region is smaller. The value of α_{down} degraded to 0.13 at 3×10^{14}n/cm^2 at 10 μA. β_{down} values were 2000-3000 before irradiation at 100 μA and degraded to 50-60 at 3×10^{14}n/cm^2.

Hughes Semiconductor has supplied NAVWPNSUPPCEN Crane with six packaged devices having several test structures bonded out from an I^2L development chip. The test chip was built using a double Schottky up-diffused process. Available for testing were a single output inverter cell, a three output, two input inverter cells, two 15 stage ring oscillators, one lateral pnp transistor, and a ten stage, divide by two frequency divider. The three output gates had all three outputs tied together and both inputs tied together. The ring oscillators included one using 0.2 mil spacing and the other 0.3 mil spacing. Two of these



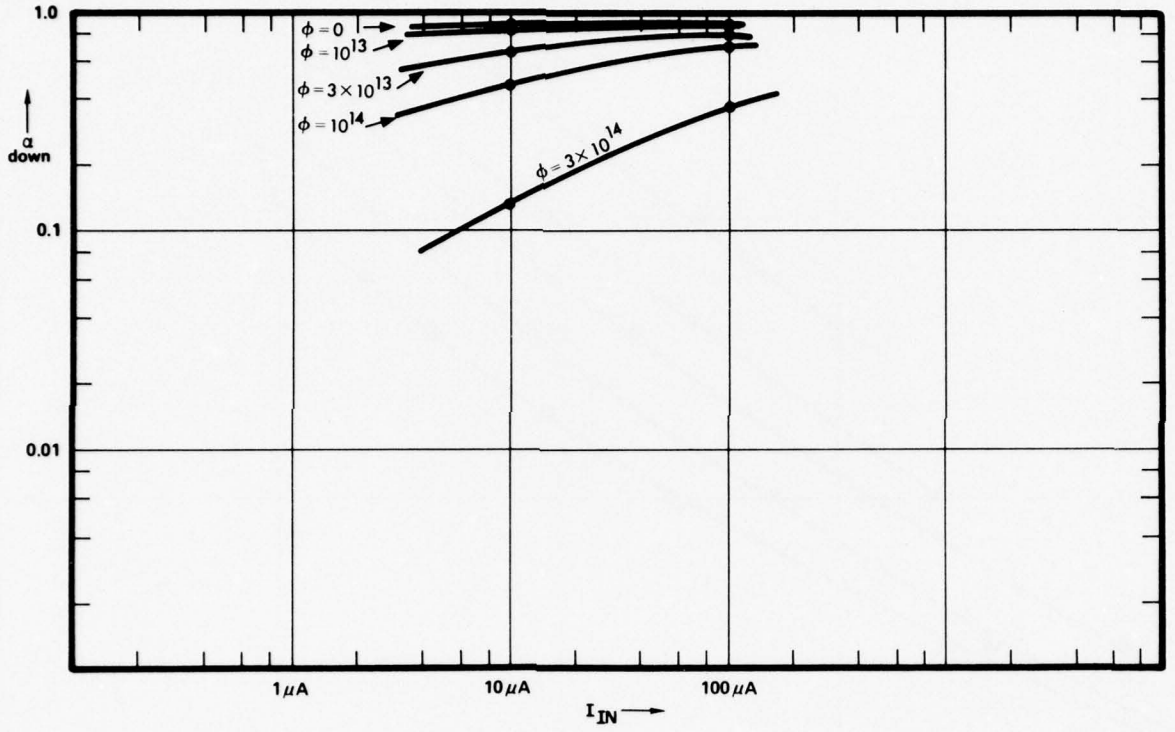
Neutron Degradation of βu vs I_C for Harris Substrate Fed Logic Development Chip

Figure 3.16



Neutron Degradation of tpd/Stage vs Total Injector Current for Harris Substrate Fed Logic Development Chip

Figure 3.17

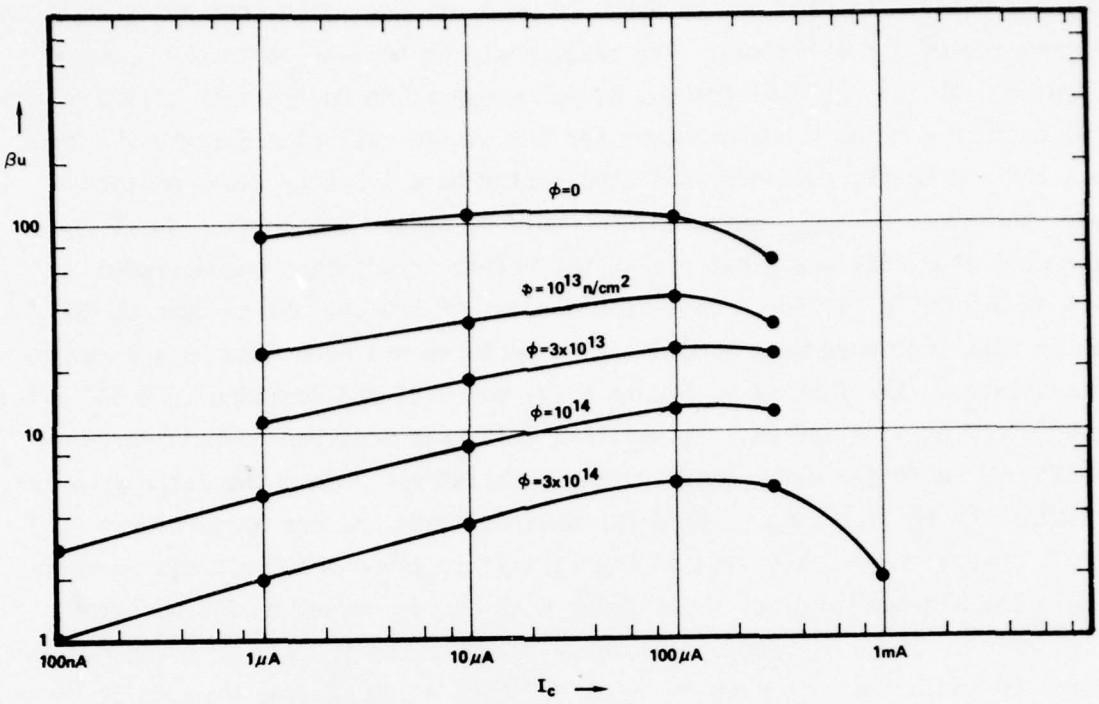


Neutron Degradation of α_{down} vs I_{IN} for Harris Substrate Fed Logic Development Chip

Figure 3.18

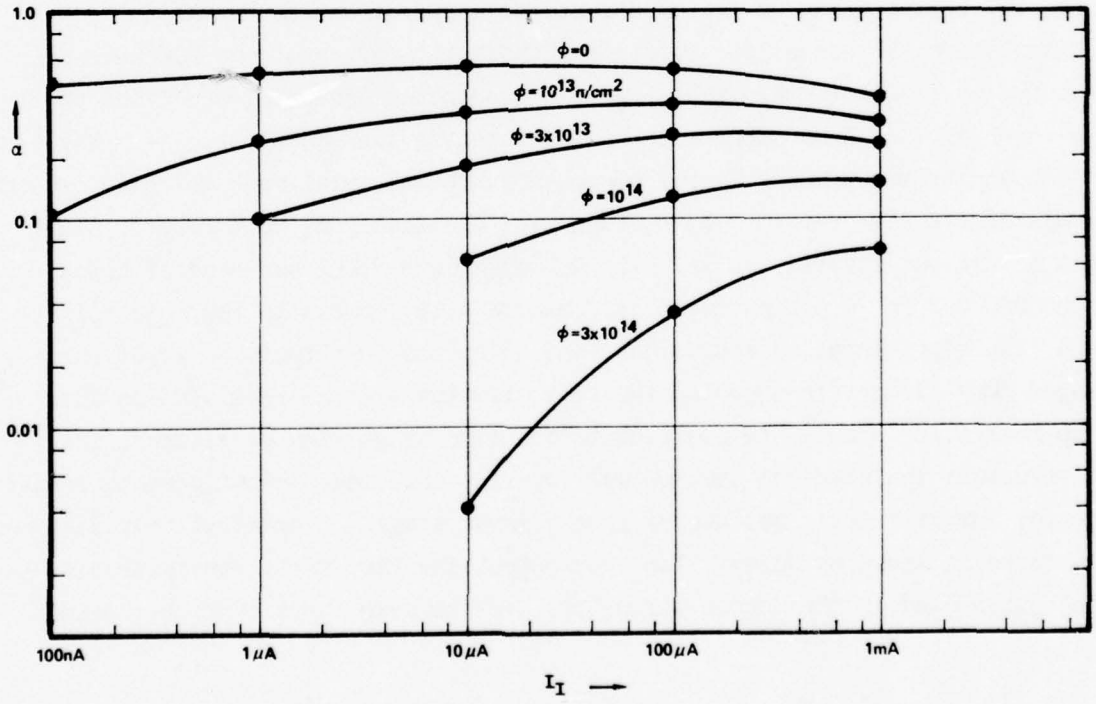
structures were irradiated on the WSMR FBR in four successive increments to a total fluence of 3 X 10^{14}n/cm^2. The results of the neutron tests are shown in Figures 3.19 through 3.21 for βu, α, and propagation delay, respectively. The βu values in Figure 3.19 are averages for the single collector structure. This device had a Schottky collector and a collector-base Schottky clamp on the output, therefore no β_{down} measurements could be made. The initial βu of the single collector cell was greater than 100 before irradiation and degraded to 5.5 at 3 X 10^{14}n/cm^2 for a collector current of 100 μA. Since none of the inverter cell injectors were bonded out, α measurements were made on a separate pnp transistor. The initial α, Figure 3.21, was 0.54 and degraded to 0.035 after 3 X 10^{14}n/cm^2 at I_I = 100 μA. Propagation delay was measured on both large (.3 mil) and small (.2 mil) geometry ring oscillators. Since the large geometry oscillators on the two samples used for neutron tests did not operate over the full current range, the data in Figure 3.21 is given for the small geometry device. The minimum prop delay was about 4 ns and decreased to 2-3 ns after 3 X 10^{14}n/cm^2. The α degradation caused a shift in the t_{pd} vs. I_I curves which resulted in an increase in prop delay at I_I/stage = 100 μA from 9 ns to 24 ns at 3 X 10^{14}n/cm^2.

The T.I. "advanced" I^2L SBP9900 chip contains a large ROM which is used for the 172 50 bit words of microinstruction. Several wafers having a metallization mask that allows electrical characterization of the ROM have been fabricated by T.I. for evaluation. T.I. has supplied NAVWPNSUPPCEN Crane one three-inch wafer of ROMs along with six packaged devices containing test structures. The test structures were derived from another special metal mask which interconnected elements of the ROM to form a five stage ring oscillator as well as providing access to various inverter cells. The ROM wafer was diced and several chips were bonded out in 24 pin packages at Crane to allow access to the injectors, ground, the eight input address lines, and 13 of the 50 outputs. Two of these packaged ROMs along with three of the test structures were irradiated on the FBR up to 3 X 10^{14}n/cm^2. In addition to the five stage ring oscillator, the test structure included one four-output inverter cell, one output geometry single collector inverter cell, and access to one input stage. Electrical test data was taken on βu, α and prop delay. The four-output inverter cell, representative of the gates used in the decode circuitry, had the base input contact located



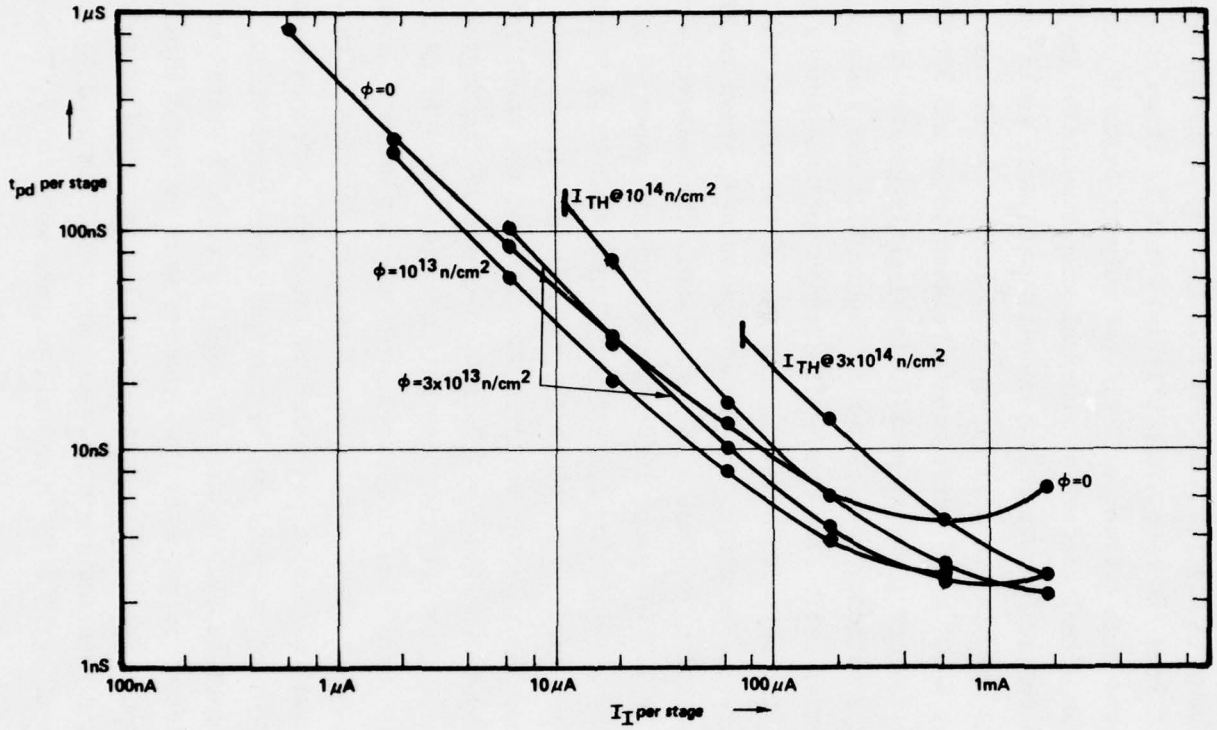
Neutron Degradation of βu vs I_C for Hughes Up-diffused I^2L Development Chip

Figure 3.19



Neutron Degradation of α vs I_I for Hughes Up-diffused I^2L Development Chip

Figure 3.20

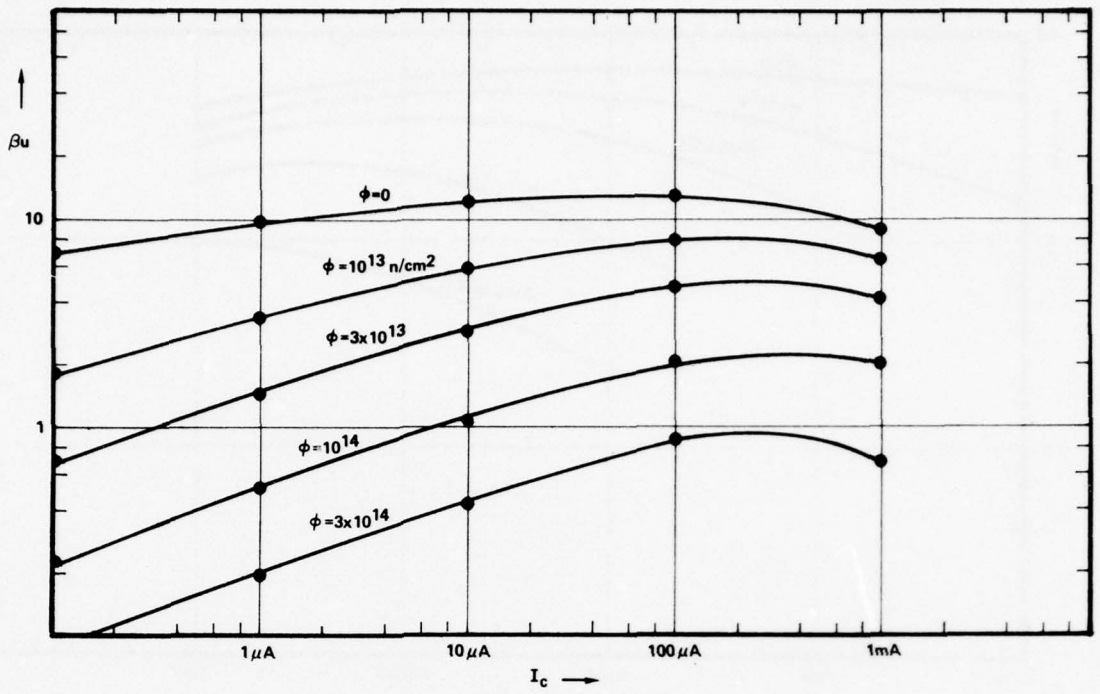


Neutron Degradation of tpd Per Stage vs I_I Per Stage for Hughes Up-diffused I^2L Development Chip

Figure 3.21

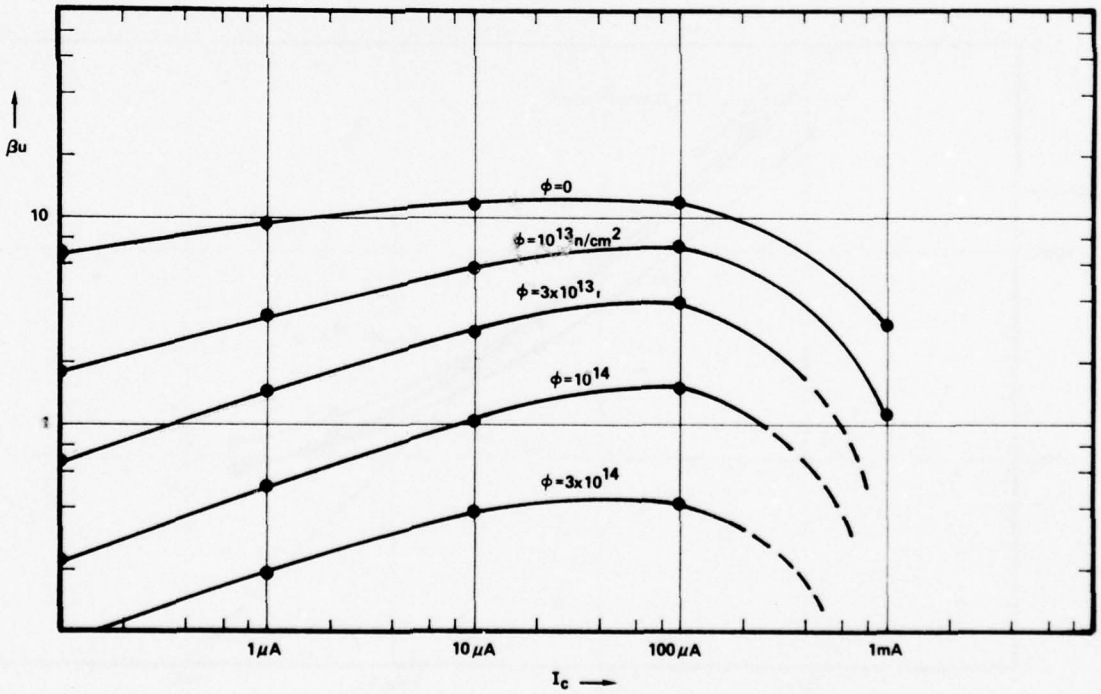
on the end of the cell farthest from the injector. The output nearest the base contact and the output nearest the injector were bonded out separately and the two center outputs were tied together and bonded out. Although the injector lead was bonded out it was also tied to eight other injectors which were feeding inoperable cells. Therefore no usable measure of α could be obtained for the four-collector cell. The results of βu vs. I_C at the various fluence levels are shown in Figures 3.22 and 3.23 for the collector nearest the base and farthest from the base, respectively. Data is shown for the two cases to illustrate the high current roll-off for outputs farthest from the current source. In an actual circuit the current source would be the injector rather than the base contact; however, the resulting roll-off would apply in the same manner. The results shown in Figure 3.23 for the worst case output give a βu of one at 1 X 10^{14}n/cm^2 for currents between 10 μA and 300 μA. The interpolated neutron failure level at peak βu is slightly greater than 2 X 10^{14} n/cm^2. The injector efficiency data, shown in Figure 3.24 was taken on the output geometry inverter cell. The open-collector output transistors have one injector feeding two outputs; however, only one of the outputs was bonded out in these structures. Therefore, the measured α values, shown in Figure 3.24 are lower than the actual α by about a factor of two. The measured α values were still above .1 at 1 X 10^{14}n/cm^2 for injector currents above 10 μA.

The prop delay vs. injector current per stage is shown in Figure 3.25 for the various neutron levels. Although the ring oscillator had only 5 inverter stages and one buffer, the injector rail fed 18 cells, so the total injector current was divided by 18 to find the I_I/stage. Because of the degradation of fanout or βu, the ring oscillators were only operable above 50 μA at 10^{14}n/cm^2. At 3 X 10^{14}n/cm^2 the ring oscillators did not operate at any current. The minimum prop delay for these samples was 8 ns. In addition to the test structures neutron tests were also performed on two ROMs. Various words of instruction were addressed and read out before and after irradiation. A pull up resistor and 1V power supply was used to read the 0 and 1 states of the 13 accessable open-collector output bits. No changes were recorded thru 3 X 10^{13}n/cm^2. At 10^{14}n/cm^2 the output high decreased and output low increased so that the difference between the high and low states was about .1V compared to .4 to .5V before irradiation. At 3 X 10^{14}n/cm^2 all outputs were "off." These tests



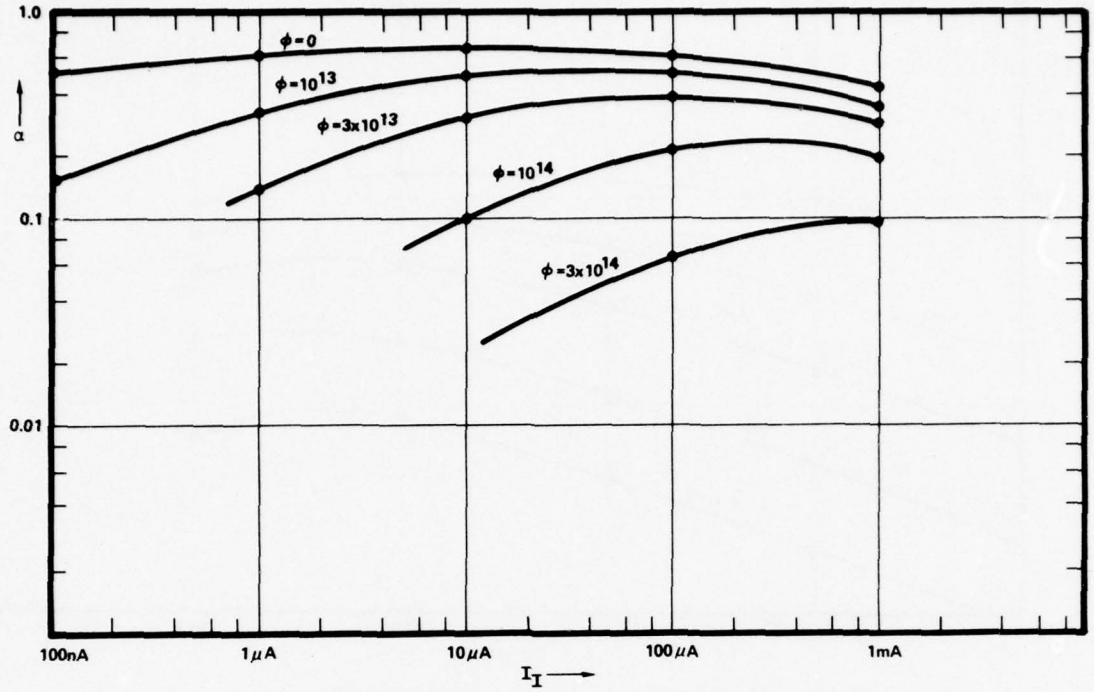
Neutron Degradation of βu vs I_C for T.I. SBP9900 Test Structures
(Collector Nearest Current Source)

Figure 3.22



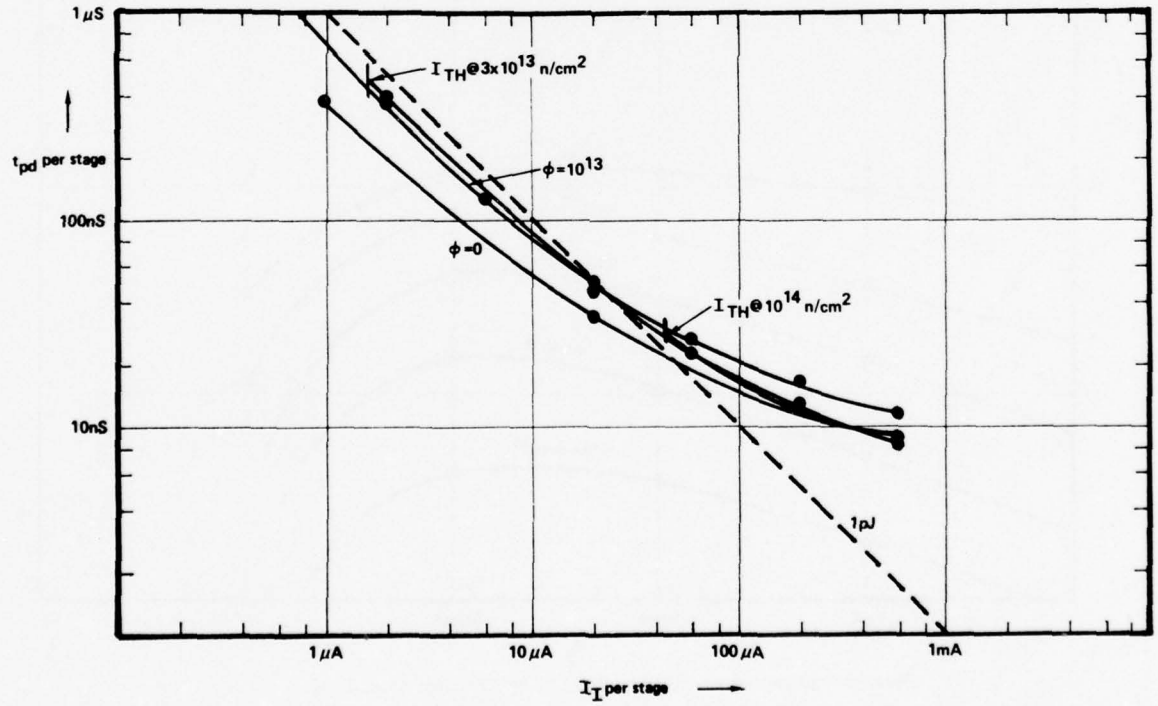
Neutron Degradation of βu vs I_C for T.I. SBP9900 Test Structures
(Collector Farthest From Current Source)

Figure 3.23



Neutron Degradation of α vs I_I for T.I. SBP9900 Test Structures

Figure 3.24



Neutron Degradation of tpd Per Stage vs I_I Per Stage For T.I. SBP9900 Test Structures

Figure 3.25

were performed at a total injector current of 25 mA which is representative of actual operating conditions in the SBP9900. This would correspond to a current per stage of 2-3 μA. The results of the ROM test are in good agreement with measurements on the test structures, appreciable degradation at 10^{14}n/cm^2 and total failure at 3 X 10^{14}n/cm^2.

3.2 LONG TERM IONIZATION EFFECTS

3.2.1 Evaluation of Long Term Ionization Effects In First Generation I^2L

The major long term ionizing radiation effects on bipolar devices are:

1. Generation of positive charge in the oxide next to the oxide-silicon interface. This positive charge consists of both fixed charge resulting from ionization effects on the interface structure and mobile positive charge from ionization of impurities.
2. Generation of fast interface states which act as recombination centers and increase the surface recombination velocity.

These two effects add to the base surface current by extending the emitter-base space charge region near the surface by depletion of p type regions and by increasing surface recombination in the neutral base regions near the surface from the radiation induced fast interface states. These effects increase the I_2 and I_6 current components shown in Figure 3.1 which act to degrade both the pnp and npn transistor gains. The increase in the base surface current from total dose for the I^2L transistors can be expected to be somewhat larger than in conventional pnp and npn transistors for the following reasons.

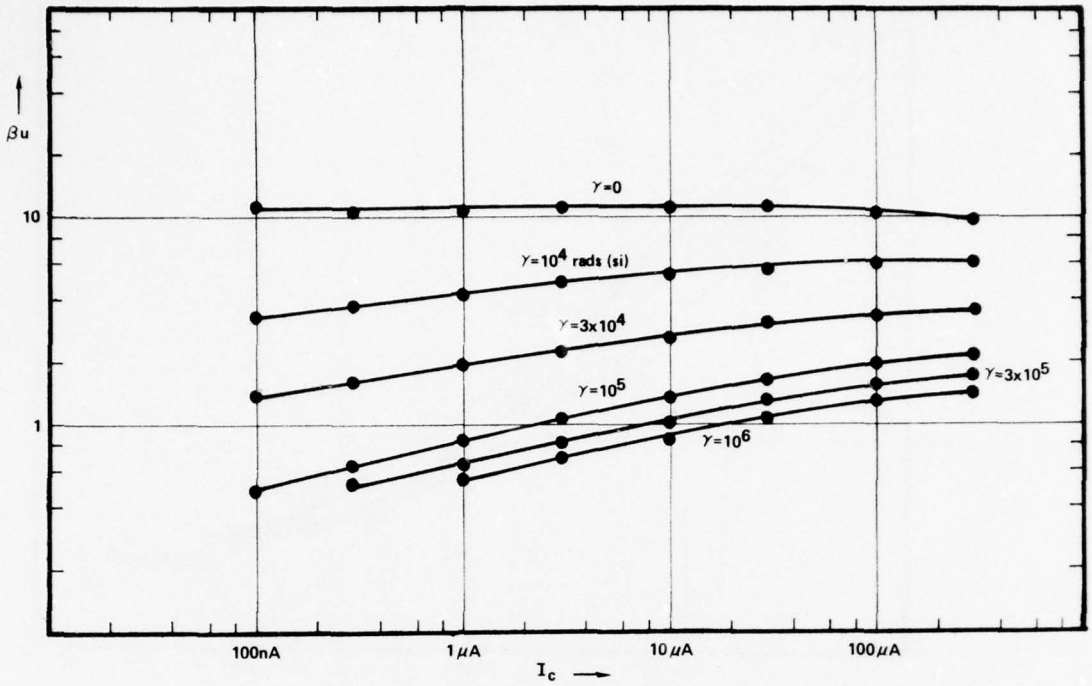
1. The lateral pnp transistor has a relatively wide base with a constant doping profile (no aiding electric field). Since the current flow is lateral from emitter to collector there is a much larger component of base current near the oxide-silicon interface than in the case of a verticle transistor. The surface recombination current is further enhanced due to the lack of an aiding electric field.
2. The vertical npn transistor has a relatively large emitter-base junction which intersects the oxide-silicon interface. Depletion of the p type base near the E-B junction at the interface will greatly enhance the space charge recombination because of the increased depletion volume. In addition there is a relatively large neutral base surface region which will contribute surface recombination current because of an increase in interface states.

Since the recombination rate is larger in the space charge region than in the bulk the ionization induced increase in base current will result in a larger percentage degradation at the lower operating currents. This increased degradation at low current has a compound effect on the cell fanout for a constant injector current because both the pnp and npn gain degradation is involved.

3.2.2 Results of Long Term Ionization Effects Tests on First Generation I^2L

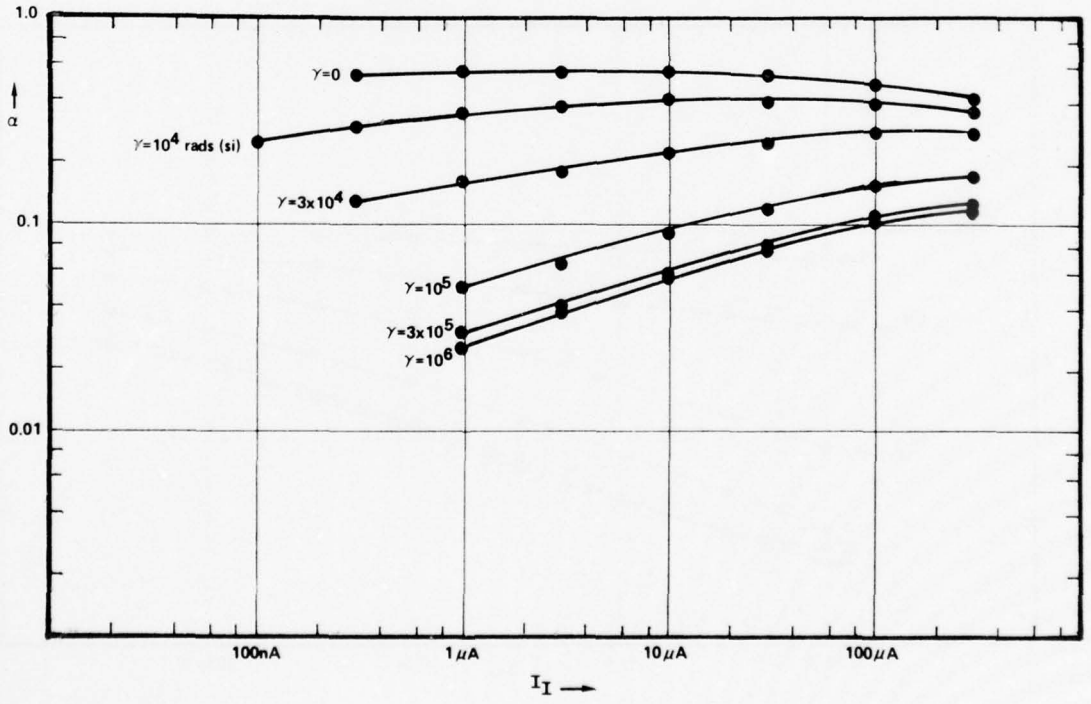
As with the neutron effects, long term ionization effects testing on "baseline" I^2L has been reported by Northrop,[24] Crane,[19,23] G.E.[28] and Boeing.[41] The Northrop data indicated operation of the ring oscillators to the highest level of exposure, 6.5×10^6 rad(Si). The average minimum operating current per stage at this exposure levels was ~3 μA. The best case inverter had a fanout of greater than 2 above 1 μA at 6.5×10^6 rad(Si). Results on the G.E. structures were given for various geometrical and doping profile configurations and the total dose failure levels ($\beta u = 1$) varied between 6×10^4 to $> 10^6$ rad(Si) at 50 μA collector current. Data taken since then on optimum geometry four-collector cells indicates $\beta u > 3$ at 3×10^6 rad (Si). The Boeing data, taken on the X0400 processor element gave a total dose failure level of 1.4×10^6 rad(Si). At this dose no degradation was measured in the output levels; however, logic errors were detected. The long term ionization data taken by NAVWPNSUPPCEN Crane on "baseline" I^2L test structures is shown in Figures 3.26 through 3.35. This data was taken on the same types of structures and the same sample sizes as shown in Table 3.1 for the neutron tests. The irradiations were performed up to 10^6 rad (Si) on a 10,000 curie Co^{60} source located at Indiana State University, Terre Haute, Indiana. All irradiations were performed with outputs reverse biased at 0.7V and the other leads grounded. Postirradiation measurements were initiated within ten minutes after exposure.

Figures 3.36 and 3.37 are summary plots of the total dose to cause a degradation of $\beta u = 1$ and $\alpha = 0.1$, respectively. The manufacturer identification codes are given in Table 3.1. As with the neutron test results, there is a wide variation in failure levels for the different vendors and all devices showed an injection level dependence on the failure level as expected. All of the devices tested operated above a threshold current level at 10^6rad(Si). This threshold varied between 8 and 50 μA collector current.



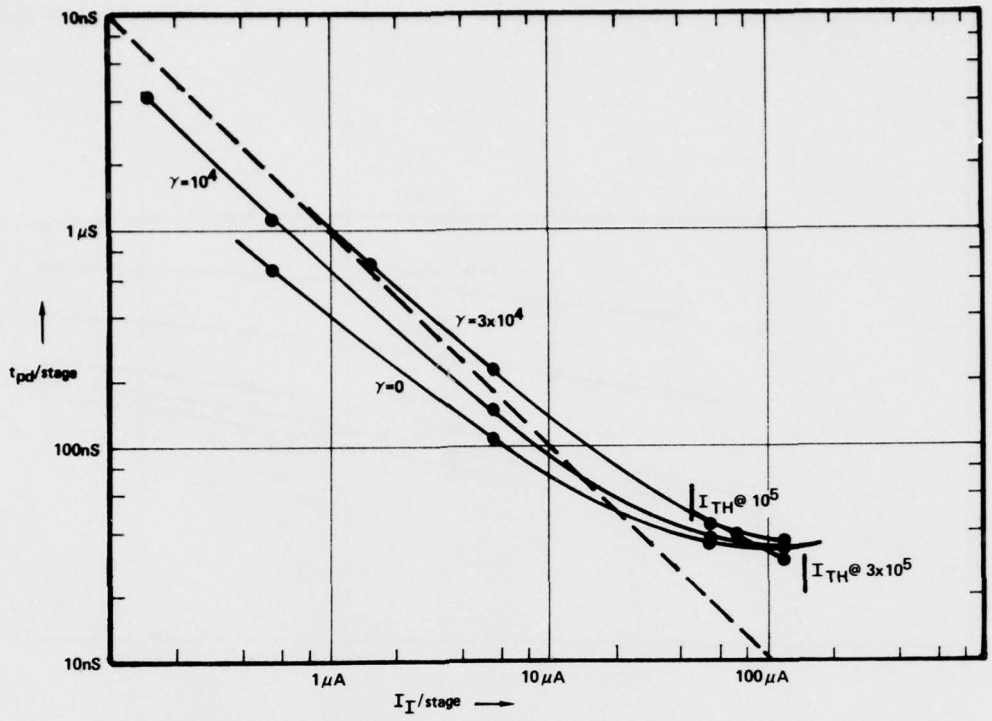
Total Dose Degradation of βu vs I_C for T.I. First Generation I^2L Development Chip

Figure 3.26



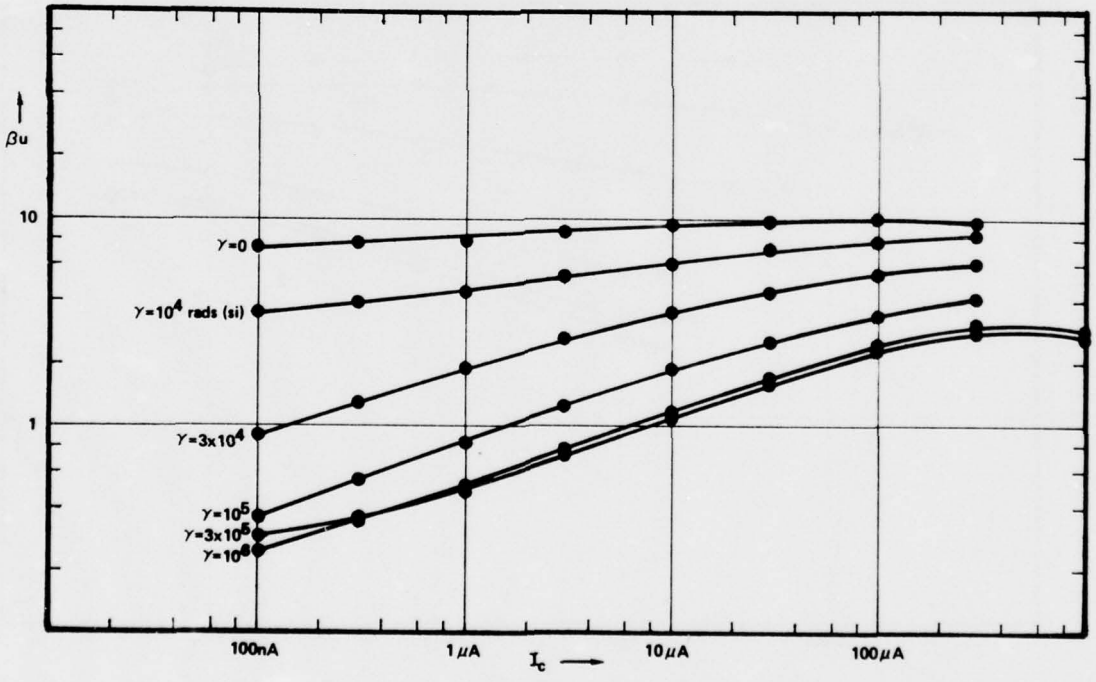
Total Dose Degradation of α vs I_I for T.I. First Generation I^2L Development Chip

Figure 3.27



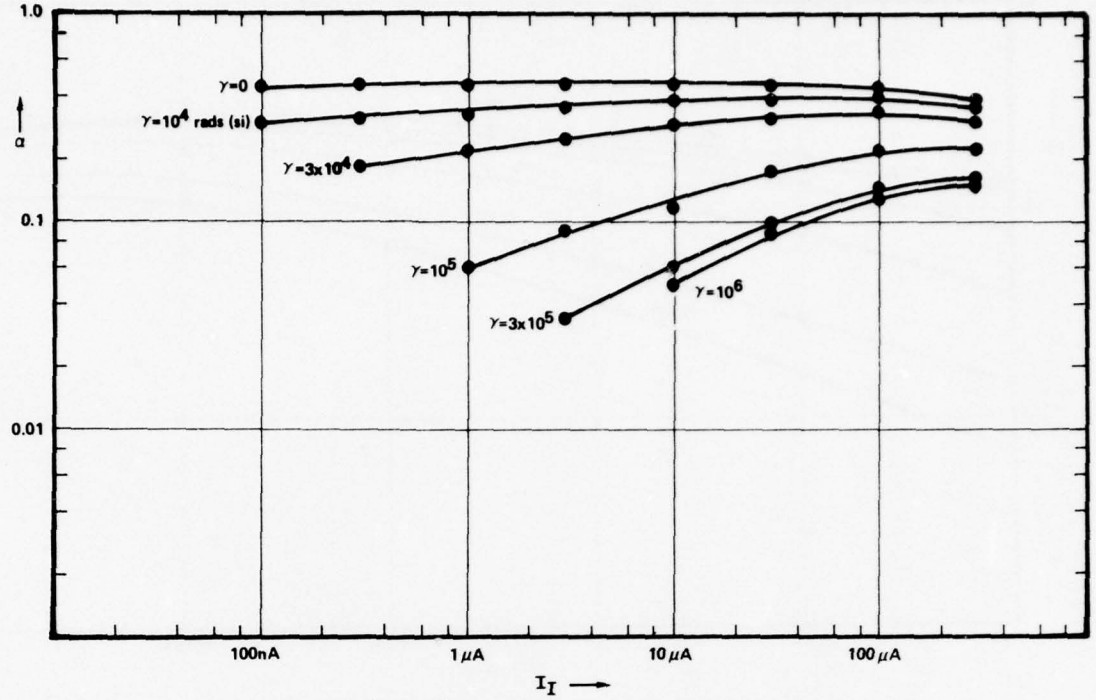
Total Dose Degradation of tpd Per Stage vs I_I Per Stage for the T.I. First Generation I²L Development Chip

Figure 3.28



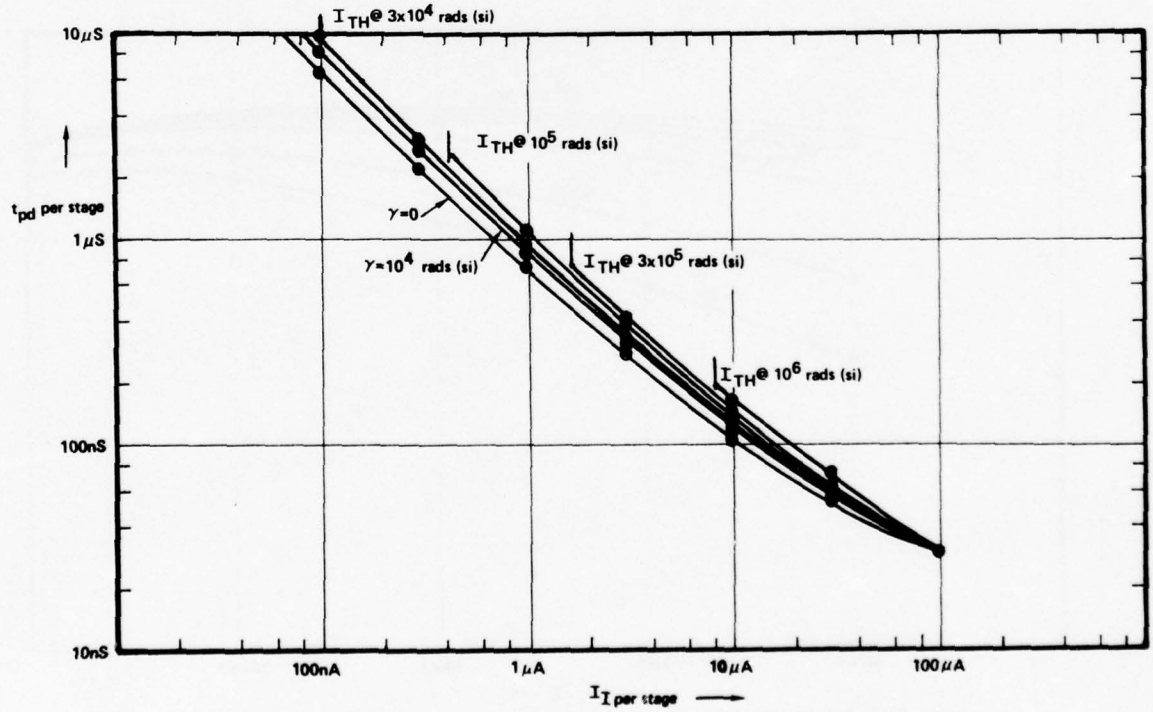
Total Dose Degradation of β vs I_C for T.I. X0400 Test Structures

Figure 3.29



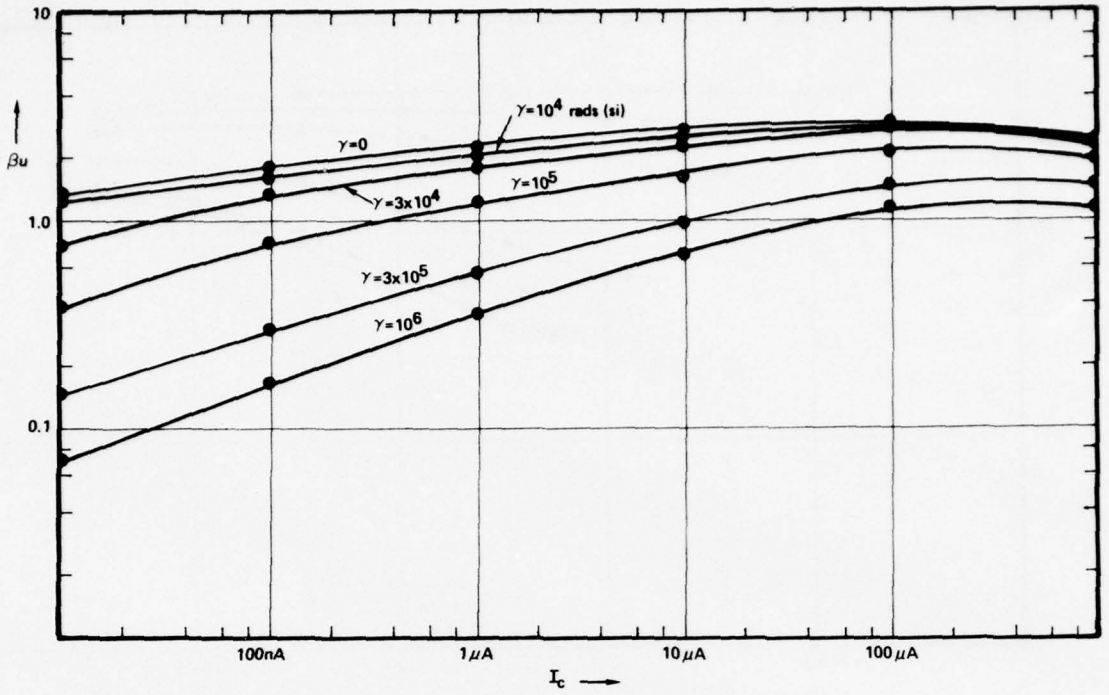
Total Dose Degradation of α vs I_I for T.I. X0400 Test Structures

Figure 3.30



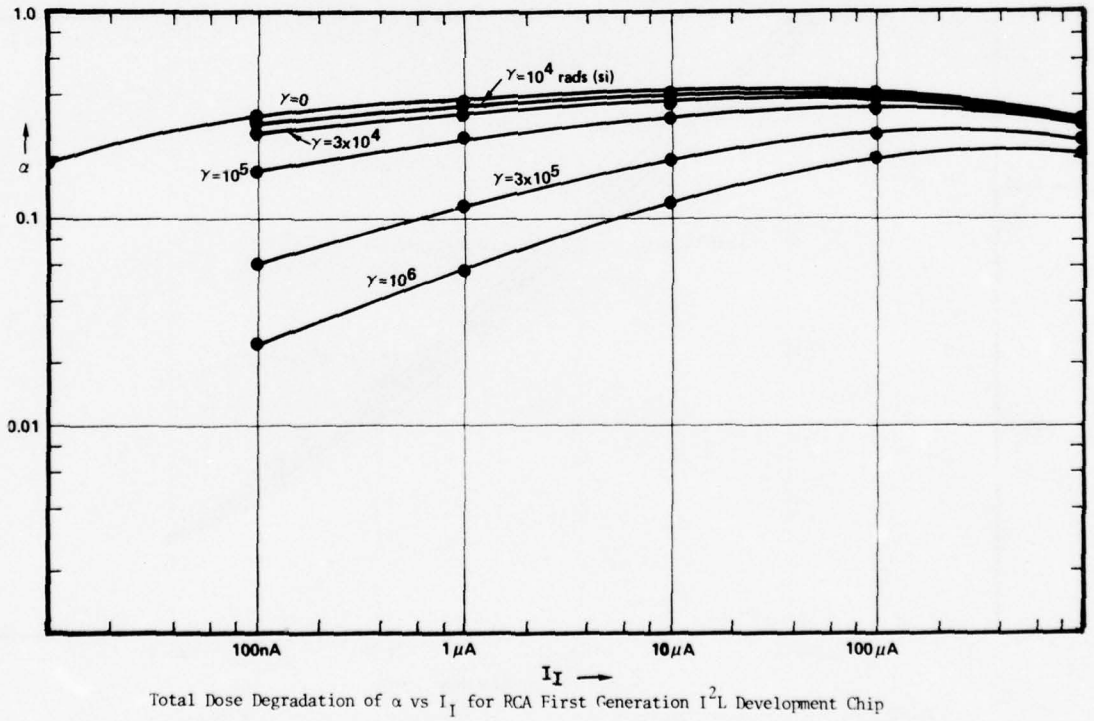
Total Dose Degradation of tpd Per Stage vs I_I Per Stage for T.I. X0400 Test Structures

Figure 3.31



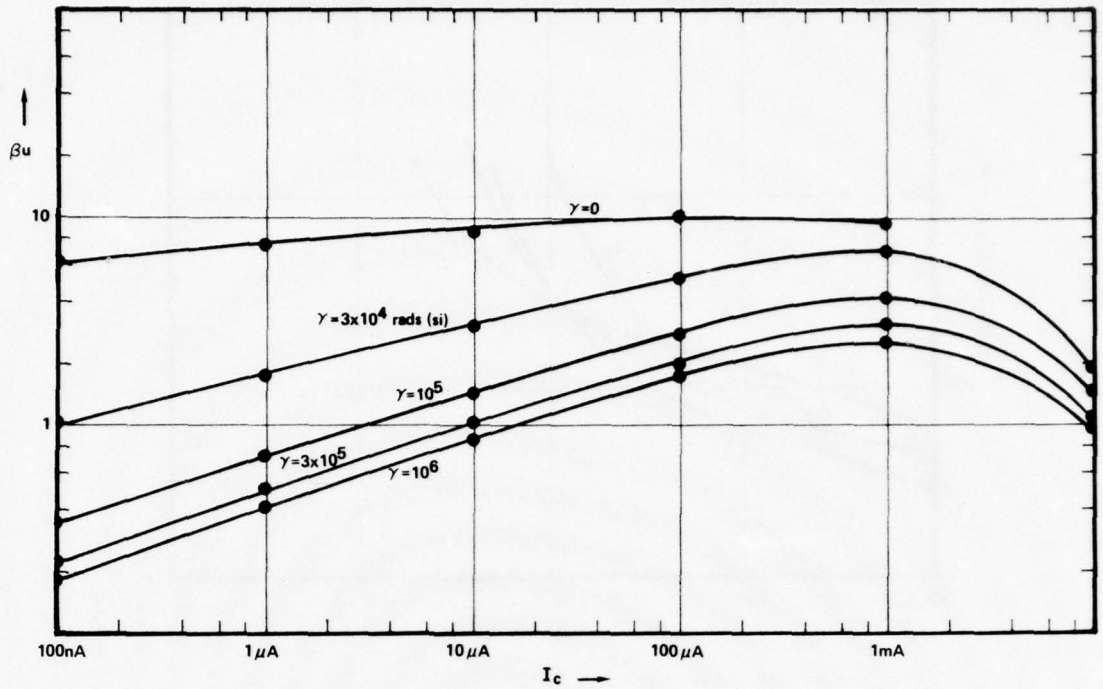
Total Dose Degradation of βu vs I_C for RCA First Generation I^2L Development Chip

Figure 3.32



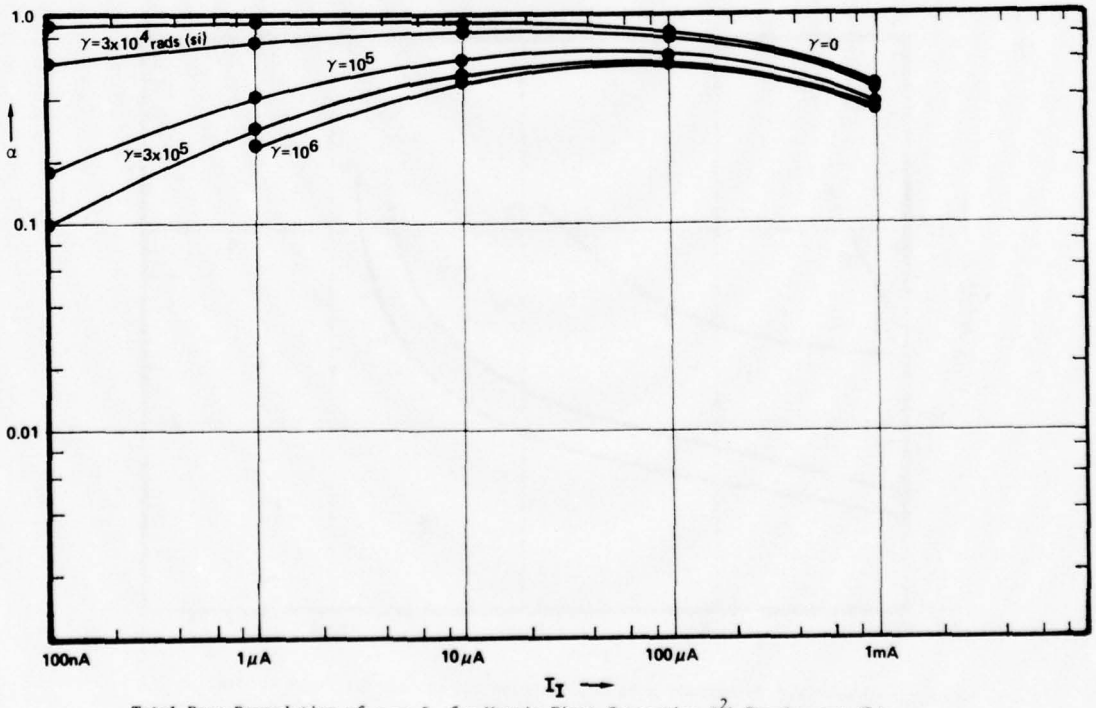
Total Dose Degradation of α vs I_I for RCA First Generation I^2L Development Chip

Figure 3.33



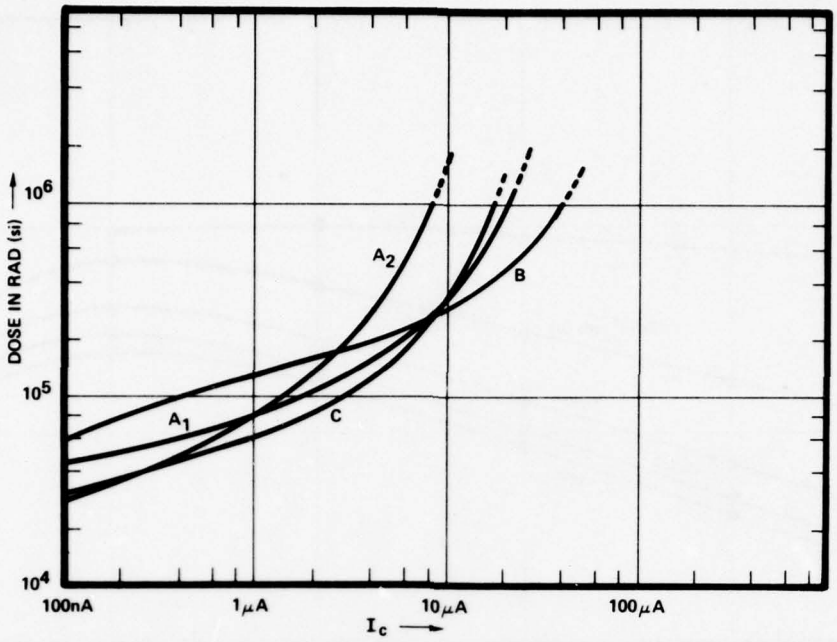
Total Dose Degradation of βu vs I_C for Harris First Generation I^2L Development Chip

Figure 3.34



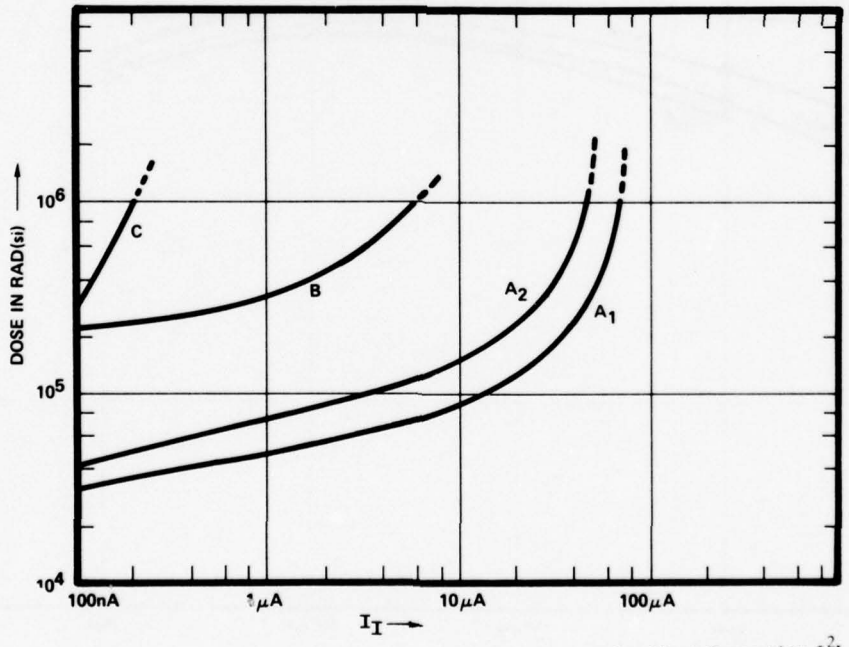
Total Dose Degradation of α vs I_I for Harris First Generation I^2L Development Chip

Figure 3.35



Total Dose Required to Degrade βu to One vs I_C for First Generation I^2L

Figure 3.36



Total Dose Required to Degrade α to 0.1 vs Injector Current for First Generation I^2L

Figure 3.37

3.2.3 Evaluation of Long Term Ionization Effects in Second Generation I^2L

Although the basic mechanisms of long term ionization effects are the same in second generation I^2L structures as they are in the "baseline" structure, the geometrical and profile variations incorporated in advanced structures will alter the net effects considerably.

In the ion-implanted structures the injector region and extrinsic base regions are deeper and higher doped. The higher doping reduces the possibility of depletion and inversion of the p regions and thus limits the spread of the emitter-base depletion region at the surface for both the pnp and npn transistors. The steeper profile resulting from the high doping should help direct current flow in the injector farther from the surface and thus decrease the amount of surface recombination in the neutral base region of the pnp transistor. Since the relatively low doping of the intrinsic npn base region helps to concentrate current flow under the collector, the amount of surface current should be reduced in the npn transistor.

In the up-diffused process utilized by ITT the lowest doping in the p region occurs at the surface. Thus in the pnp, higher current density occurs at the surface. For this reason, considerable increases in base surface current would be expected for both the pnp and npn structures. In the Hughes up-diffused structure, however, the extrinsic base regions are heavily doped and resemble, along with the injector, the doping profile of the ion-implanted structures. The same arguments which apply to the ion-implanted structure would apply to the Hughes up-diffused structure.

In the substrate fed logic structure all critical surface areas are minimized. The emitter-base junction of the pnp injector only contacts the silicon surface at the edges of the chip which is essentially out of the active region. The npn emitter-base junction intersects the top surface only where contact is made to the n epi ground plane with a deep n+ diffusion. Although the p epi doping is relatively low, extrinsic base surface current flow is reduced by the use of a vertical injector. However, because of the relatively low doping of the p epi there is a greater possibility of inversion which could cause high leakage between outputs or from output to ground. This is handled in the Harris SFL process by a shallow p+ diffusion into the top surface of the p epi.

In p epi I^2L the pnp structure is double diffused. The injector is heavily doped which will minimize the spread of the emitter-base surface depletion region into the injector. Also the base surface area in the pnp is very small and the doping profile is directed such as to minimize base current flow at the surface. The npn transistor has a relatively low doped p epi base region similar to substrate fed logic. There is a greater possibility of emitter-base surface depletion spread into the base than in structures with highly doped extrinsic base regions. Also there is a possibility of output to output or output to ground channeling unless a highly doped p region is deposited on the surface of the p epi, as with SFL.

One consideration which has not been addressed for second generation I^2L total dose effects is the use of oxide isolation. Most I^2L manufacturers propose using some form of oxide isolation (Isoplanar, V groove, anodic, etc.) and one manufacturer, Fairchild, has oxide isolated devices in production. The use of oxide isolation can adversely effect the total dose hardness because the quality of the interface between the silicon and the isolation oxide is not as good as the top surface interface. The use of oxide isolation greatly increases the npn base surface area and exposes the npn emitter-base depletion region to the isolation oxide. Preliminary data taken by Fairchild on isoplanar test structures indicate relatively low total dose hardness levels. The adverse effect of the isolation oxide can be offset by a highly doped n region adjacent to the isolation as would be the case in substrate fed logic.

3.2.4 Results of Long Term Ionization Tests on Second Generation I^2L

Total dose tests have been performed on T.I. ion-implanted, Hughes up-diffused and Harris substrate fed I^2L test structures. The data on SFL was taken by Harris[36] on a Co^{60} source both passively and with the units under operating conditions (injectors forward biased). Measurements were made on βu of the npn, β_{down} of the pnp and minimum speed-power product. The results are summarized below in Table 3.2.

Table 3.2

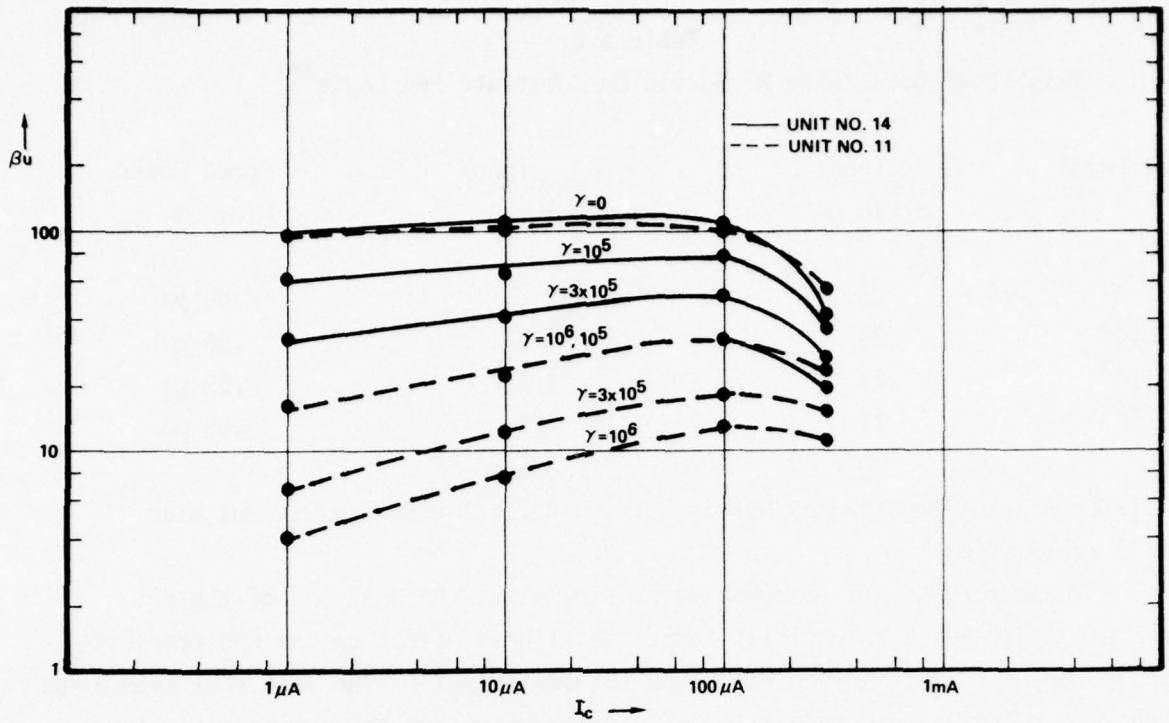
Total Dose Data Taken By Harris On Substrate Fed Logic[36]

Dose Level	β_{up}(npn) at 10 μA	β_{down}(pnp) at 10 μA	Speed Power Minimum
0	25	12	.05 pJ
10^5	23	7.5	.05 pJ
5 X 10^5	22	5.5	.05 pJ
10^6	21	4.5	.05 pJ

No difference was reported by Harris between devices with and without bias during irradiation.

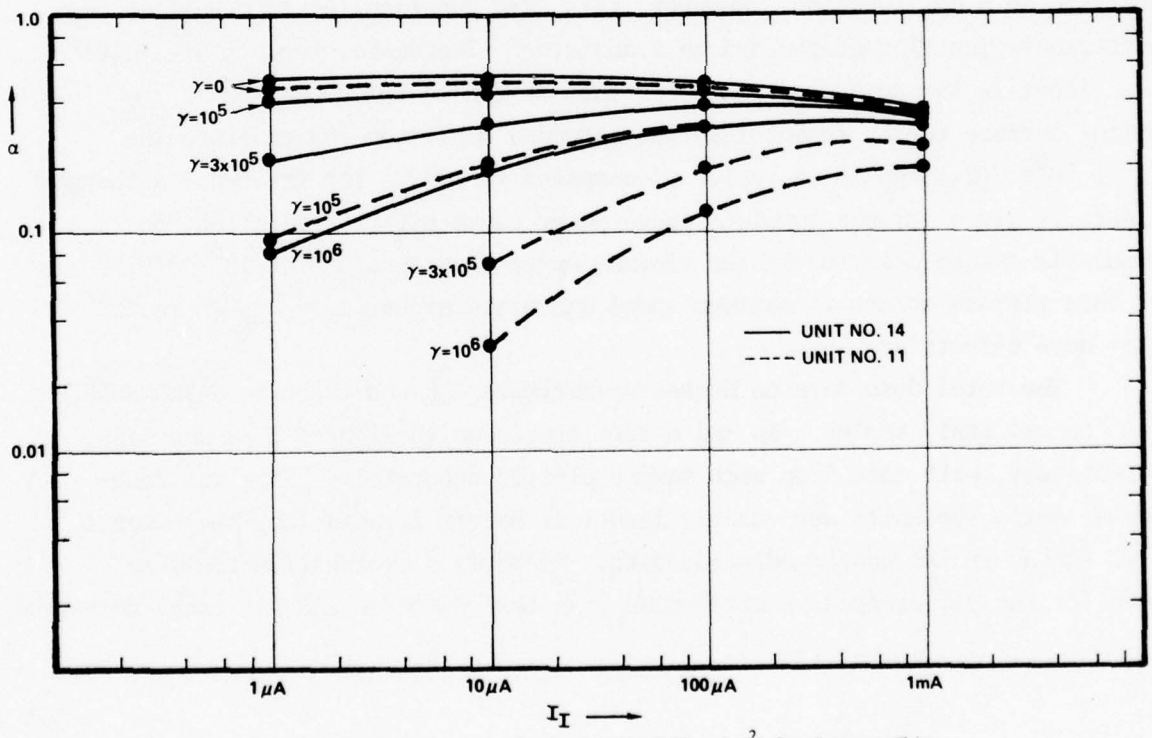
These results are somewhat surprising since the analysis of the SFL structure indicated a potentially larger total dose effect on the npn transistor than on the pnp. This may be explained to some extent by the fact that measurements on the pnp injector were made with the p epi rather than the substrate as the injector. When measuring β_{down} for the pnp, the surface of the emitter-base depletion region occurs at the p epi to n+ ground contact junction rather than the substrate to n epi junction. However, this same junction (n+ to p epi) is the emitter-base junction of the npn up transistor. Therefore, the primary total dose effect in the down pnp transistor must be due to recombination in the emitter surface region rather than the extended depletion region since the ΔI_B at 10^6rad(Si) and 10 μA is 1.4 μA compared to .08 μA for the npn. Although no data is given for the complete speed-power curve after irradiation, no measurable change occurred in the minimum speed-power product at 10^6rad(Si). In SFL this minimum occurs at maximum speed and hence higher currents where the total dose effects are less.

The total dose data on Hughes up-diffused I^2L was taken by NAVWPNSUPPCEN Crane on two test samples. βu and α data are shown in Figures 3.38 and 3.39, respectively, with data from each sample plotted separately. This was done because while the units were nearly identical before irradiation, there was a large spread in the postirradiation data. No obvious explanation could be found for the differences. Irradiation bias test fixtures and data were rechecked



Total Dose Degradation of βu vs I_C for Hughes Up-diffused I^2L Development Chip

Figure 3.38



Total Dose Degradation of α vs I_I for Huphes Up-diffused I^2L Development Chip

Figure 3.39

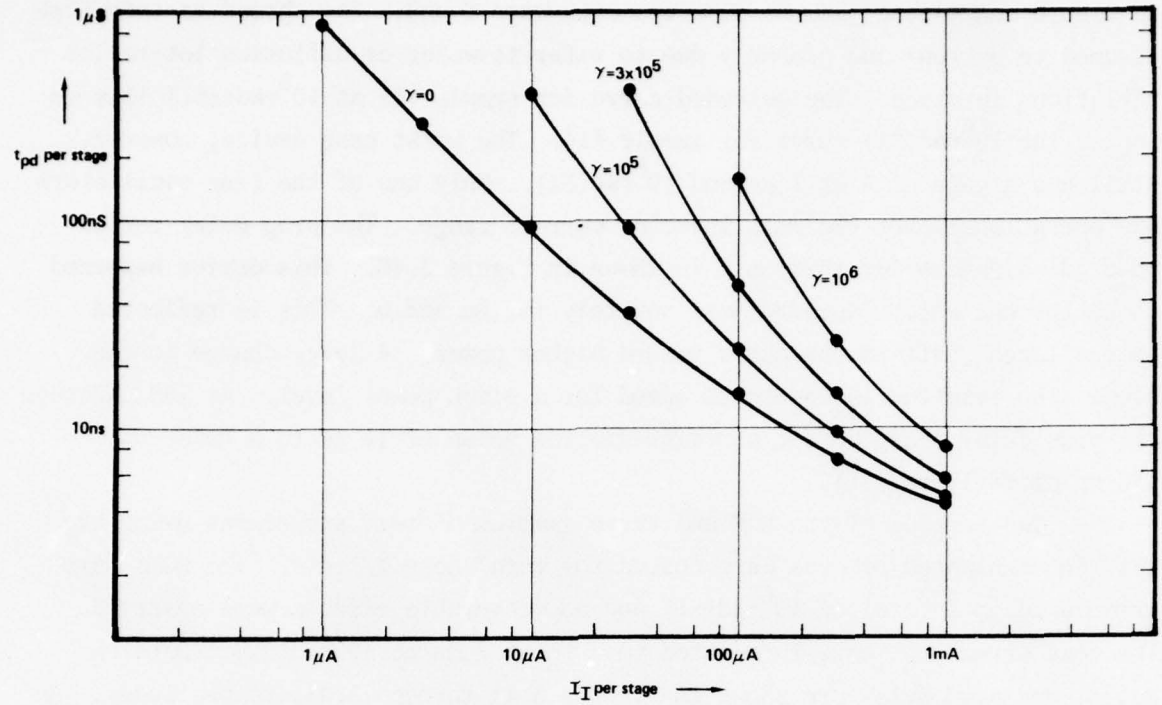
to assure consistency and no discrepancies were found. The spread is therefore assumed to be real and probably due to wafer-to-wafer or diffusion lot-to-lot variations in oxide. The degraded curve for sample #11 at 10^5rads(Si) lies on top of the 10^6rad(Si) curve for sample #14. The worst case device, however, still has a gain of 4 at 1 μA and 10^6rad(Si). Only one of the ring oscillators was operational over the full injector current range. The prop delay versus power dissipation for this unit is shown in Figure 3.40. This device happened to be the one which degraded more severely for βu and α. This is reflected in the large shift in the curve toward higher power. A large change in the slope also resulted in increased speed for a given power level. At 100 μW/stage the prop delay changed from a preirradiation value of 14 ns to a value of 150 ns after 10^6rad(Si).

Two samples of the ROM and three samples of test structures using the T.I. ion-implanted process were tested for total dose effects. The ROMs were irradiated to a total of 10^6rad(Si) and no measurable effects were observed. The test structures were irradiated to a total dose of 10^7rad(Si). Data on βu, α, and prop delay are shown in Figures 3.41 through 3.43, respectively. βu data is shown on the four-output gate for the collector nearest to the current source. As with the neutron data the α is shown for the output geometry structure. The measured α was about half the actual α since the injector was feeding two bases only one of which was pinned out. The speed-power curve on these devices was nearly unchanged down to 1 μA/stage at 10^6rad(Si) and the ring oscillators were still operating at 10^7rads(Si). βu was greater than one at 10^7rad(Si) for operating currents above 500 nA.

3.3 TRANSIENT IONIZING RADIATION EFFECTS

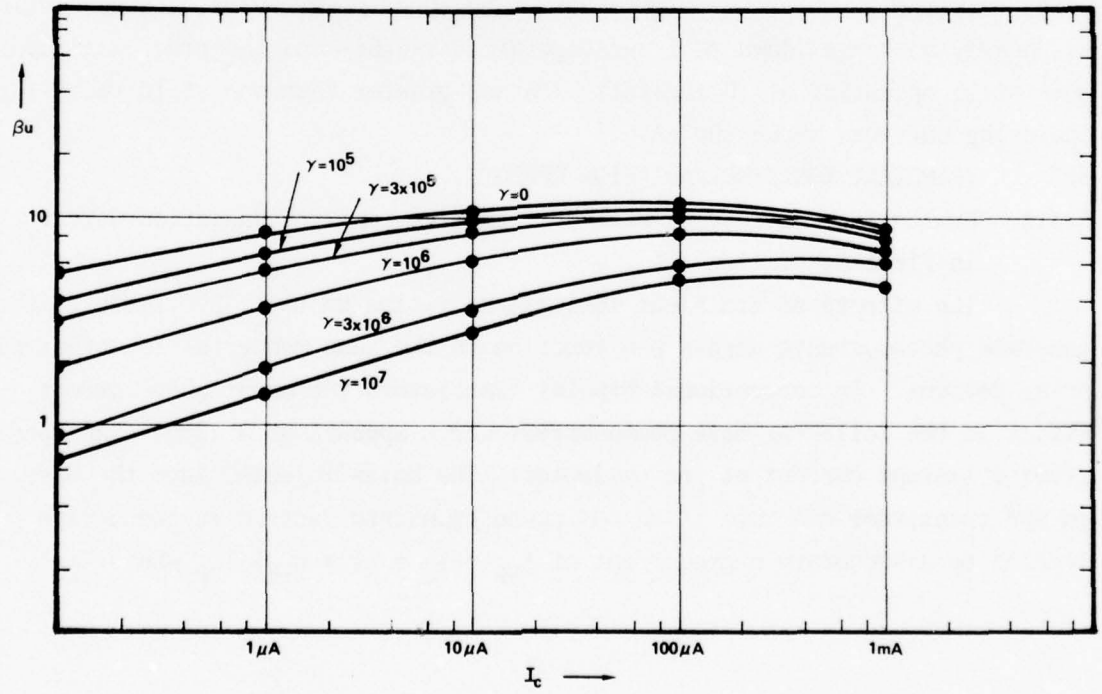
3.3.1 Evaluation and Test Results of Transient Ionizing Radiation Effects in First Generation I^2L

The effects of transient ionizing radiation on the I^2L structure is to generate photocurrents across p-n junction in the same manner as for other bipolar devices. In conventional bipolar transistors the major photocurrent effect is the collector-base photocurrent which appears as a large transient reverse leakage current at the collector. The holes injected into the base of an npn transistor can turn it on and cause transistor action in the device leading to a secondary photocurrent of $I_{SP} = I_c = (1 + h_{FE})\ I_{PP}$ where I_{PP}



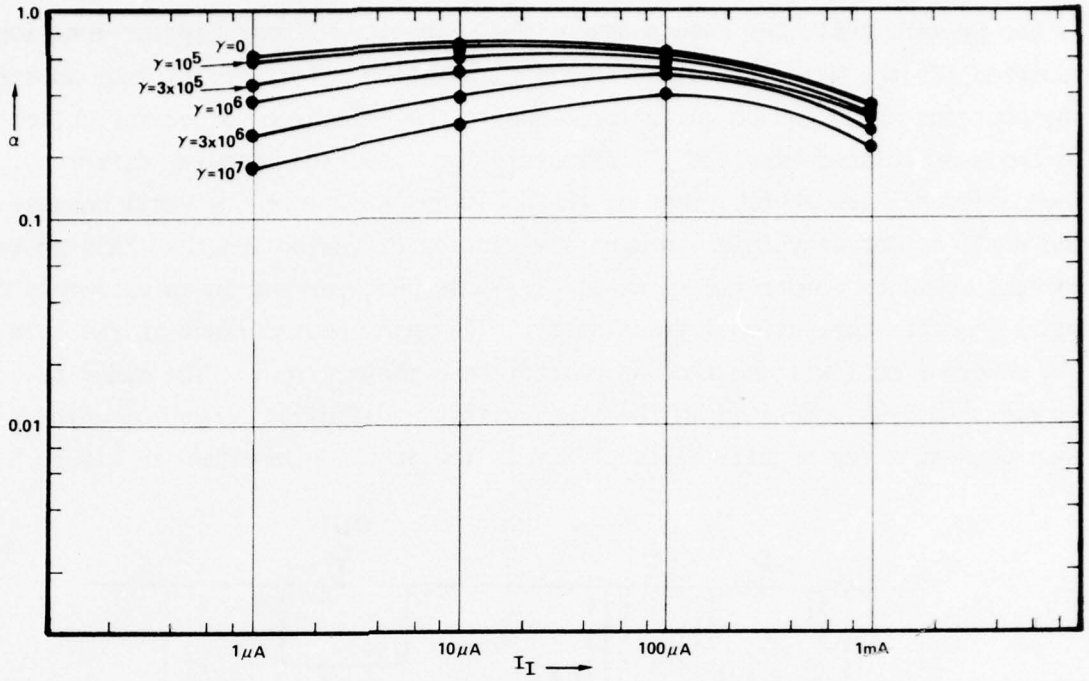
Total Dose Degradation of tpd Per Stage vs I_I Per Stage for Hughes Up-diffused I^2L Development Chip

Figure 3.40



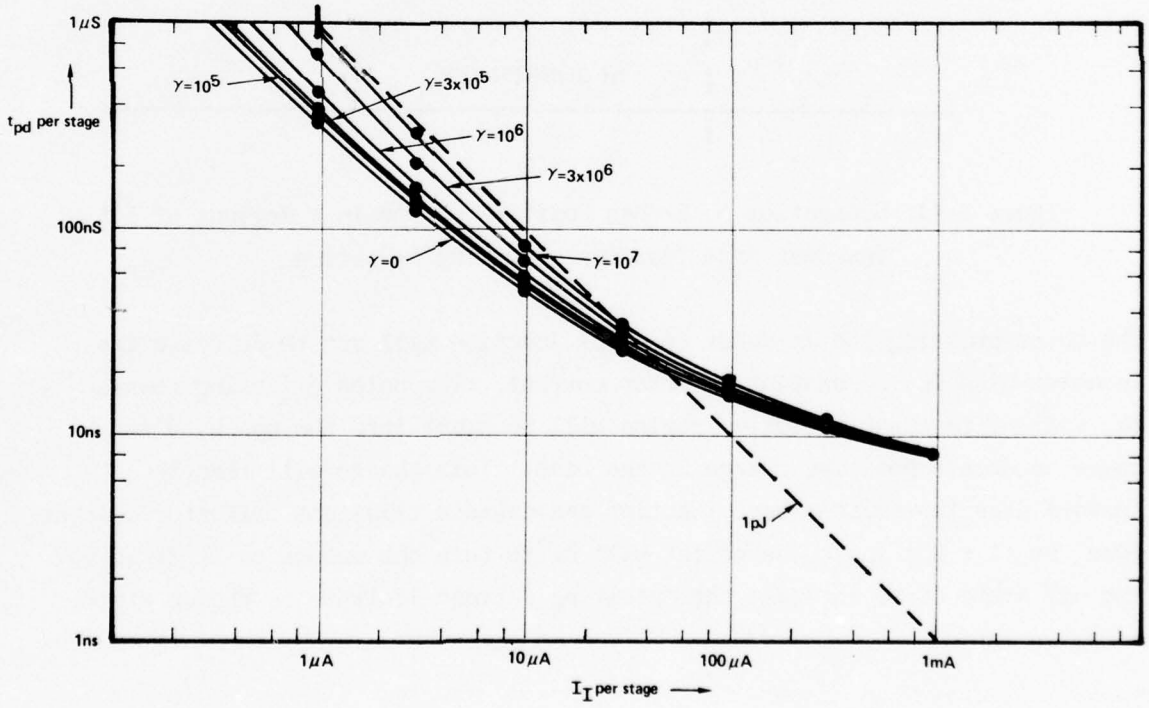
Total Dose Degradation of βu vs I_C for T.I. SBP9900 Test Structures

Figure 3.41



Total Dose Degradation of α vs I_I for T.I. SBP9900 Test Structures

Figure 3.42



Total Dose Degradation of tpd Per Stage vs I_I Per Stage For T.I. SBP9900 Test Structures

Figure 3.43

is the primary collector base photocurrent. In conventional bipolar junction isolated ICs the major transient ionizing radiation effect arises from substrate photocurrent which can be quite large due to the effective volume for collection. In the non-isolated baseline I^2L structure the situation is quite different. The collector-base photocurrent of the npn transistor is quite small because of the small depletion volume and minority carrier diffusion lengths (this photocurrent would be comparable to an emitter-base photocurrent in an extremely small geometry conventional transistor). The major photocurrent in the baseline I^2L inverter cell will be the npn emitter-base photocurrent. The minority carriers (holes) generated in the n epi within a diffusion length of an n-epi to p depletion region will be swept across the junction as shown in Figure 3.44.

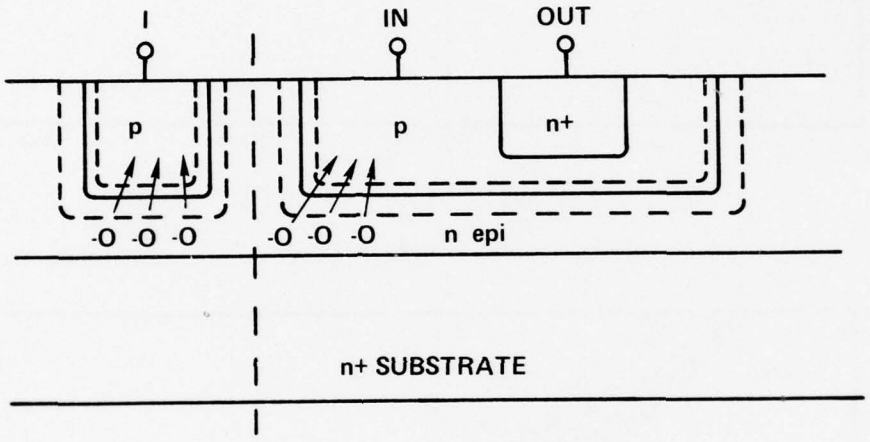


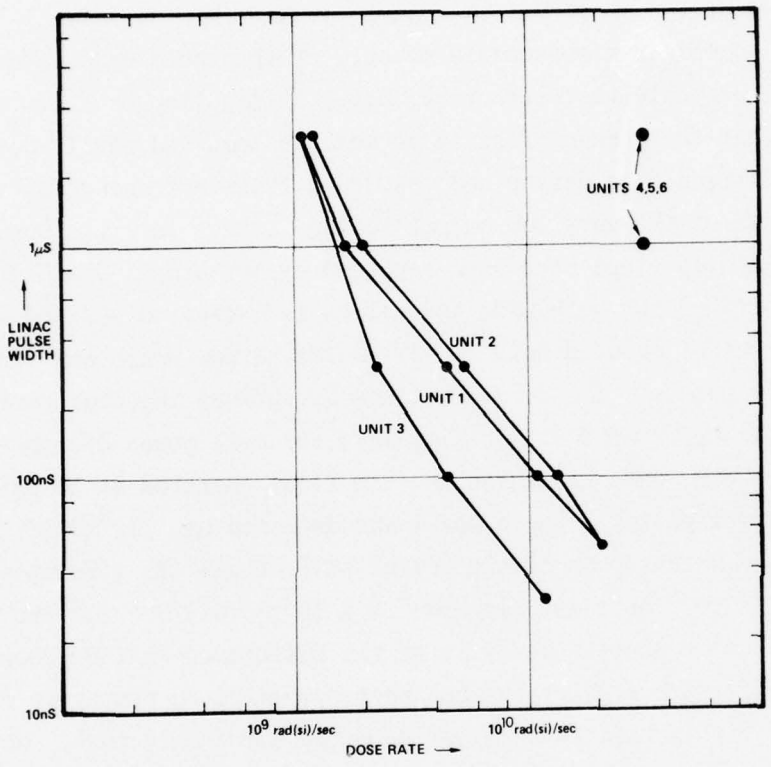
Figure 3.44 Generation of Excess Positive Charge In P Regions of I^2L Inverter From Transient Ionizing Radiation

The holes crossing the injector to n epi junction will act to decrease the injector bias for a constant injector current. The holes diffusing toward the npn emitter-base depletion region will be swept into the npn base and cause an excess positive charge in the base. This charge will tend to forward bias the emitter-base junction and cause a transient collector current equal to $(1 + \beta u)\ I_{PP}$. The effect will be to turn the output on if it is in the off state or to increase the operating current if it is in the on state.

In a complex logic array there will be numerous competing photocurrents generated in the various inverter cells. A complete analysis of transient dose rate upset would have to include the layout, geometry, diffusion profiles, biases and carrier lifetimes of the various inverter cells of the array. Dose rate upset levels for individual inverter cells on development chips would be of little value in predicting the upset for arrays because the cells in an array are so closely packed that adjacent cells will be competing for carriers generated in the n epi.

In order to obtain a reasonable measure of threshold dose rate upset on I^2L devices, a bistable test structure, e.g., a flip flop or shift register, is desirable so that the change of state is well defined and easily detected. It is much more difficult to define and measure a transient change of state in an inverter because of the very low output voltage swings in I^2L. Dose rate upset tests on I^2L flip flops have been reported by Northrop[24] and G.E.[28] The Northrop data was taken for both wide and narrow radiation pulses and indicated thresholds for upset of about 5×10^9 rad(Si)/s for narrow pulse and $2\text{-}3 \times 10^9$ rad(Si)/s for wide pulses. The data was taken at various injector current levels and indicated logic upset of $2\text{-}4 \times 10^9$ rad(Si)/s for cell power dissipation as low as 32 μW. The G.E. data was taken on flip flops operated at 50 μA/gate using a Flash X-Ray (narrow pulse). Logic upset was detected at $\sim 10^9$ rad(Si)/s. Recent unpublished data by Northrop on 32 bit serial shift registers gave upset levels of $\sim 5 \times 10^8$ rad(Si)/s for the first bit and $\sim 5 \times 10^9$ rad(Si)/Sec for the remaining bits. Although a comprehensive analysis of the difference in the observed upset difference in the first bit upset has not been completed, a tentative explanation is that the first bit is tied to a larger geometry input structure. No latchup has been observed by either Northrop or G.E. in any of their dose rate tests on I^2L devices.

The only baseline I^2L test chips characterized by Crane having a bistable circuit were the RCA devices containing dual D flip flops. These units were tested on the White Sands Missile Range LINAC facility. Six samples were tested at different LINAC pulse widths using 20 MeV electrons The devices were operated at an injector current corresponding to the minimum propagation delay. Figure 3.45 is a plot of the dose rate threshold for a change of state vs. the radiation pulse width. All six devices were supposedly from the same



Dose Rate Upset Threshold vs LINAC Pulse Width for RCA I^2L Flip Flops

Figure 3.45

diffusion lot, but the data is grouped into two groups of three each with a spread of greater than an order of magnitude between groups. No explanation has been found for the apparent discrepancy. The devices were encapsulated in epoxy DIPS making failure analysis extremely difficult. The packages were X-rayed to guarantee that the same structures were bonded out on all six chips. This was done because the chip had two dual flip flop test circuits using different cell structures.

3.3.2 Evaluation of Transient Ionizing Radiation Effects in Second Generation I^2L

Although preliminary test structures of several second generation I^2L processes have been characterized in neutron and total dose environments, no transient ionizing radiation tests have been performed to date. NAVWPNSUPPCEN Crane has plans for dose rate tests on ion-implanted up-diffused and SFL in March or April 1977. In addition to the lack of test results, no detailed analytical analysis has been performed for transient ionizing radiation effects on either baseline or second generation I^2L. The discussion pertaining to photocurrent effects on baseline I^2L addressed only the principle components of photocurrent in an individual inverter cell. The overriding effects of competition for carriers between adjacent cells, and cancellation of photocurrents between cells can only be addressed for a specific circuit, layout and process. A few comments can be made, however, about the relative magnitude of the various photocurrents within an individual inverter cell for the second generation structures.

In the ion-implanted structure from T.I. the n epitaxial region is greatly reduced because of the thinner epi. The npn emitter-base photocurrent must arise from holes generated in the small volume epi region or the highly doped n+ substrate. In either case this photocurrent will be very small. The only other photocurrent components which contribute to the turn on of the npn base (and thus gives rise to the npn secondary photocurrent) would be injection of holes from the npn collector. The collector area, however, is quite small. Therefore, the photocurrent in this structure may be assumed to be lower than for the baseline structure.

For the up-diffused structure the npn collector region will contribute significantly to the excess hole charge in the base since the collector to base area ratio is larger than in other structures, especially where Schottky

collectors are used. The pnp collector-base photocurrent will also contribute to this excess hole charge. The contribution from the npn emitter will be negligible, however, because of the high doping of the substrate. Secondary photocurrent will be much larger because of the higher current gain ($\beta u > 100$).

The nature of the dose rate effects in the p epi structure will be quite different than for the baseline structure since there is very little n volume to inject holes into the base of the npn. The n+ substrate and n+ collector diffusions will contribute very little because of the low minority carrier lifetimes in these regions. The major source of excess positive charge in the npn base will arise from electrons generated in the base crossing both the collector-base and emitter-base junctions. If the p epi thickness is much smaller than the baseline process n epi thickness, then the dose rate upset level would be expected to be smaller.

In SFL the excess positive charge in the npn base will be nearly equally contributed by electrons leaving the p epi and holes leaving the n epi. The total charge should be comparable to that of a baseline structure with an n-epi thickness equal to the combined n and p epi thicknesses for the SFL structure.

Some considerations which have to be made concerning dose rate effects on actual I^2L devices which have not been addressed for the individual inverter cells are:

1. Photocurrent effects from isolation regions for junction isolated devices.
2. Photocurrent and latchup in the input/output interfacing structures.

For I^2L structures having minimal dose rate response the primary transient dose rate upset may be determined by the interfacing. Although Latchup has not been observed on baseline I^2L, and analysis indicates that no voltages appear in I^2L circuits of sufficient amplitude to sustain a latch condition, the possiblity of latchup must be considered if Schottky T^2L interfacing is utilized.

3.4 ELECTRICAL PULSE OVERSTRESS

Burn-out can occur in semiconductor devices either from high dose rates or EMP-generated voltage and current pulses. Large electrical pulses can cause either metallization or junction burn-out but the predominant failure mode in most ICs is junction burn-out. Because of the small geometry of the I^2L cells, the possibility of burn-out from internally generated photocurrents from high dose rates is small. The only experimental data published to date on high dose

rate effects is that of G.E.[28] Flash X-Ray tests on I^2L test structures at 10^{12}rad(Si)/s resulted in no catastrophic failures. The major susceptibility of I^2L to electrical pulse overstress will be EMP- or IEMP-generated transients occurring at input and output interfaces. Commercial I^2L LSI circuits may be quite vulnerable to electrical pulse overstress, especially at the input terminals. The power supply and ground terminals should not be particularly susceptible because of the large number of elements connected to a common pin, sharing the electrical overstress energy. Protection against electrical overstress at the input/output interfaces, however, will require either multistage large geometry I^2L buffering or some form of isolated I^2L using T^2L buffers.

3.5 SUMMARY OF RADIATION EFFECTS DATA ON I^2L

Radiation effects characterization data has been presented on several first and second generation I^2L processes in both neutron and total dose environments. A very limited amount of dose rate data has been taken on first generation I^2L. No data has been taken to date on electrical pulse overstress. A summary of the neutron and total dose data is presented in Table 3.3 in bar chart form comparing the various I^2L processes. The bar chart brackets the observed and projected degradation of I^2L test structures and devices based on the data taken by Crane, Northrop, G.E. and Boeing. The ranges of degradation are given for moderate damage (significant changes in α and βu), failure at low operating currents ($\beta u \leq 1$ for $I_C \leq$ 1-10 μA) and failure at maximum speed (I_C = 100 μA - 1mA). Some liberty has been taken in projecting the damage ranges to low operating currents in the cases where data was only recorded for the higher currents and in projecting failure levels for high neutron or total dose levels above the highest radiation test levels. In several cases the test structures or devices were only irradiated to 10^6rad(Si) total dose and no failures occurred. The highest total dose level for which data has been taken is 10^7rads(Si), therefore no projections have been made above this level. Although no neutron data has been taken above 3 X 10^{14}n/cm^2, reasonable projections of failures levels can be made based on damage coefficients calculated at lower levels.

The neutron data summarized in Table 3.3 indicates that neutron failure levels of up to 10^{15}n/cm^2 can be achieved at maximum operating speed (100 μW - 1 mW per gate power dissipation). On the other hand without attempting to optimize either the βu or neutron damage coefficients, baseline I^2L can fail at fluence levels in the 10^{12}n/cm^2 range.

There is also a wide variation in the total dose response of various I^2L processes. While some baseline processes were observed to degrade severely in the 10^4 - 10^5rad(Si) range other baseline processes degraded only moderately at 10^6rad(Si). All of the second generation structures tested showed moderate or very little degradation at 10^6rad(Si) even at bias currents as low as 100 nA per gate. However, none of the total dose data taken on I^2L processes included oxide isolation. Based on analysis and preliminary data by Fairchild, the total dose failure levels for oxide isolated structures may be very low (10^4 - 10^5rad(Si)).

The dose rate data, all of which has been taken on baseline I^2L devices, is summarized in Table 3.4.

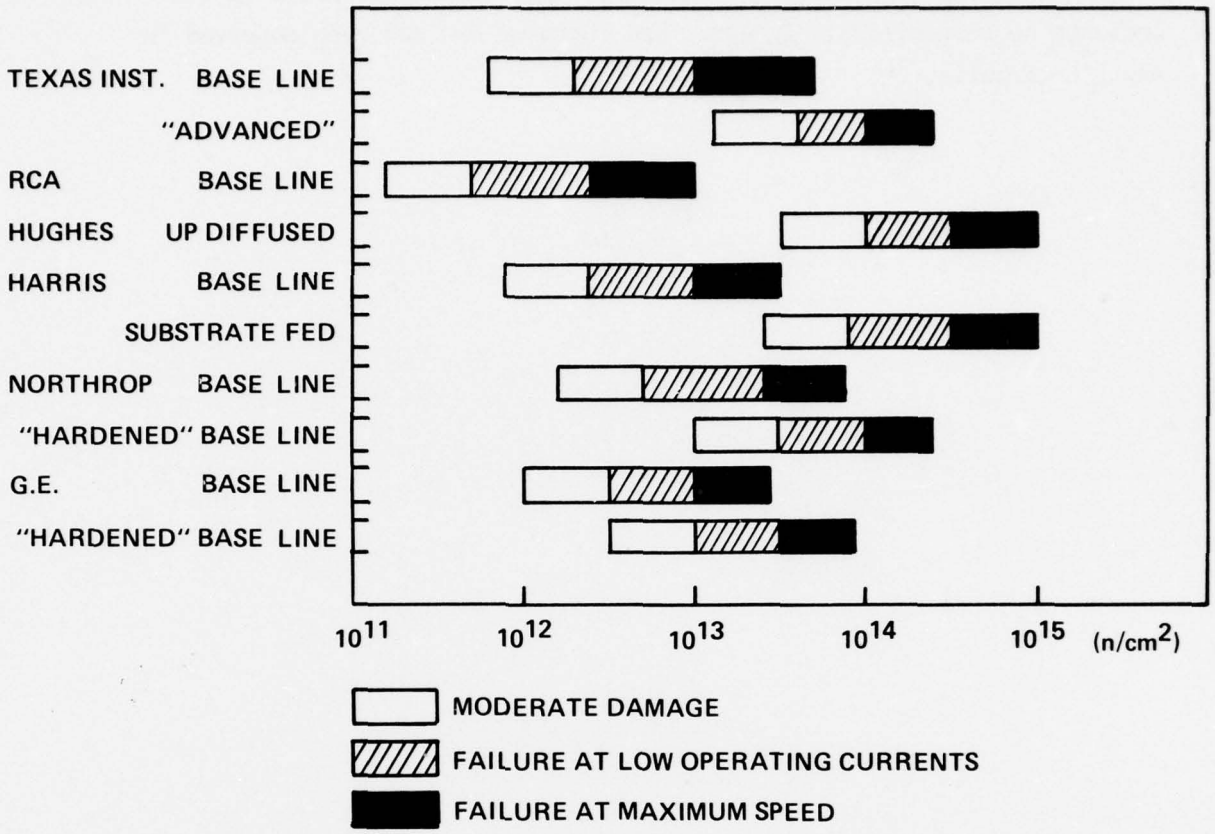
Table 3.4 Summary of Transient Ionizing Radiation Data On I^2L

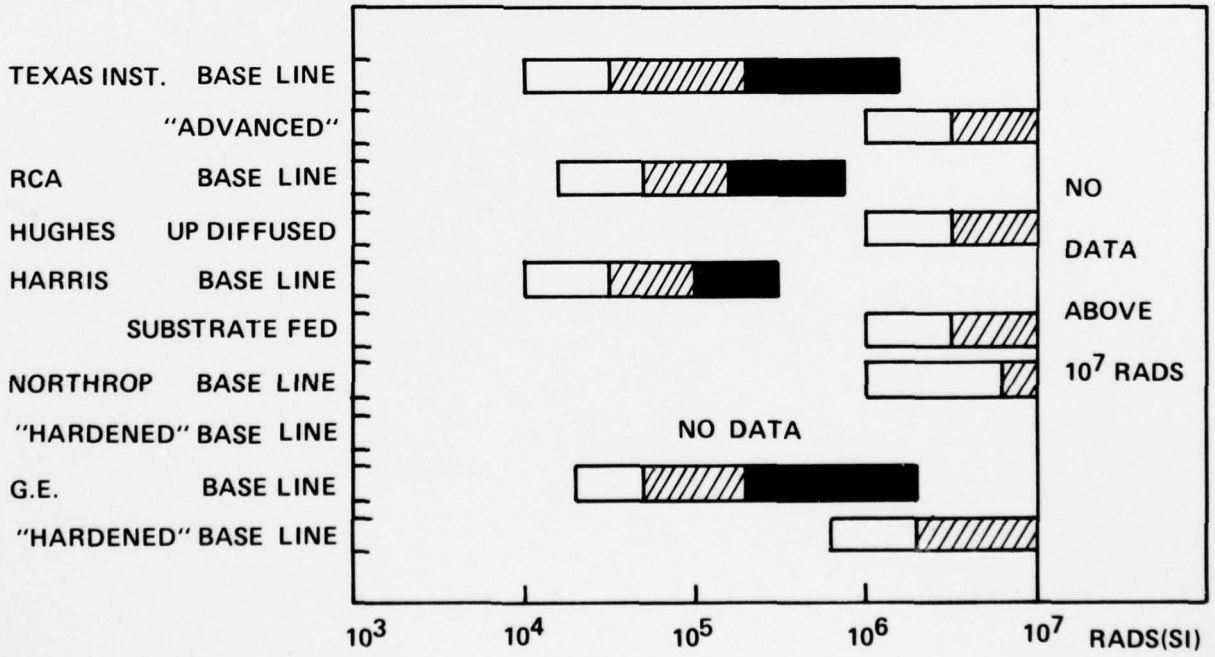
VENDOR/TEST DEVICE	DOSE RATE UPSET LEVELS Rad(Si)/Sec	
	Narrow Pulse	Wide Pulse
RCA/Flip Flops	10^9-10^{10}	$2X10^8$-$3X10^9$
T.I./SBP0400	———	$2.1X10^7$
Northrop/Flip Flops	3-$5X10^9$	2-$3X10^9$
Northrop/Shift Registers	$5X10^{8*}$-$5X10^9$	———
G.E./Flip Flops	10^9	———

*Low Upset On First Bit Only

The need for more extensive dose rate upset data on actual LSI I^2L arrays is apparent from the data taken by Boeing on the SBP0400. While data on flip flops and shift registers indicates upset levels of 10^9 - 10^{10}rad(Si)/s, the dose rate upset levels of large arrays may be much lower because of pattern or layout sensitivity.

Table 3.3 Summary of Neutron and Total Dose Degradation of I^2L





The only high dose rate (10^{12}rad(Si)/s) tests performed on I^2L indicate no castastrophic failure, and latch-up has not been observed in any I^2L circuits.

SECTION 4

TRADEOFF EVALUATION FOR RADIATION HARDENED I^2L

4.1 GENERAL CONSIDERATIONS

An evaluation of the tradeoffs for radiation hardening I^2L is a many faceted problem. Consideration must be given not only to the tradeoff between radiation hardness and device electrical performance but also the tradeoffs involved between hardening in one environment vs. other environments and between hardness and processing complexity (hence yield and cost). The question of what variations of the geometry, process variables and structure serve to increase the radiation hardness of I^2L has been discussed to some extent in Section 3 both by analysis and preliminary experimental results. The question of manufacturing complexity and producibility is much more difficult to answer since the answer depends very much on the individual manufacturer involved. A process for which one manufacturer routinely achieves high yields and good reliability may be extremely difficult for other manufacturers. The question of electrical performance is dependent not only on the functional and performance specification for the actual device but how the device is used in an actual system. For instance a fairly high speed processor element which demonstrates good neutron hardness at optimum speed may fail at much lower neutron levels if used for slow, very low power applications.

An additional consideration for radiation hardened military I^2L is the commercial base of the process. It appears from the trends in second generation I^2L that the baseline process will only be used for very low power applications where speed is not a consideration and in applications where the I^2L logic is combined with linear devices on the same chip. For applications such as real time signal processing and data processing that requires higher speed, some form of second generation I^2L will be the commercial base. Two highly likely candidates for commercial fast I^2L are the ion-implanted and up-diffused processes. Based on the results of the military systems LSI applications study, the major use of I^2L LSI devices will be in the data and signal processing areas where speed is essential. Unless military system program offices are willing to develop and maintain unique I^2L structures which have no commercial base, then the direction of fast commercial I^2L will have a definite impact.

4.2 RADIATION HARDENING TRADEOFFS FOR FIRST GENERATION I^2L

4.2.1 Neutron Hardening

Neutron hardening of first generation I^2L is achieved by minimizing the gain degradation of both the lateral pnp and inverted npn transistors. The gain degradation follows the well know relation

$$\frac{1}{\beta_\phi} - \frac{1}{\beta_o} = \Delta\ 1/\beta = K\phi$$

where β_o and β_ϕ are the initial and degraded gains and K is a damage coefficient. Maximum post irradiation βu can be achieved by increasing the initial gain and/or reducing K. In the case of the pnp transistor the major parameters affecting gain are the base width and n-epi (base) doping. Unfortunately both of these variables also effect the gain of the npn transistor. Decreasing the n-epi doping level improves pnp gain by increasing the minority carrier lifetime in the base. However, this decreases the gain (βu) of the npn primarily because of the degradation of emitter efficiency. Decreasing the base width of the pnp also increases the pnp gain and reduces the neutron damage coefficient (which is proportional to the neutral base region volume). However, this reduction in pnp base width increases the lateral back injection from the npn base to the n-epi which reduces the βu of the npn. Because of these interdependencies, there is tradeoff involved between βu, α (pnp gain), and pnp damage coefficient for both epi resistivity and pnp base width which must be optimized for hardness and performance. Another major variable is the epitaxial thickness. The epi thickness must be maintained fairly large (5-10 μm) if linear devices are to be built on the same chip. This is necessary to maintain proper breakdown voltages for the linear devices. For totally I^2L devices, the best performance and hardness is obtained by minimizing the epi thickness. Minimizing the epi thickness can create problems in process control and yield, however, it will improve α, βu and reduce K.

The npn base width can be minimized in order to improve βu and switching speed. There is however, an optimum value for base width since further reduction will lead to low BV_{CEO}, process control problems, and increased

lateral base resistance which can cause high-current gain fall off at lower current levels. The n+ collar around the p diffusion reduces the lateral injection of holes from the base and injector region and thus improves the gain of both the npn and pnp transistors. The maximum benefit is obtained with an n+ collar which extends to the substrate. The tradeoffs involved are an increase in the npn emitter-base depletion capacitance which adversely affects the low current switching speed and the addition of a processing step which could affect yield.

The use of an oxide collar rather than an n+ collar increases gain in the same manner without introducing additional depletion capacitance. The limitations with this approach are the complexity of the additional processing and the possibility of reduced total dose hardness because of the addtional oxide-silicon interface.

4.2.2 Total Dose Hardening

The total dose hardness of baseline I^2L is affected by p type surface doping concentrations, base surface areas, emitter-base depletion surface interface areas, and oxide processing variables. A reduction in total dose degradation of baseline I^2L can be achieved by higher surface p doping concentrations, minimum base surface areas, minimum emitter-base junction surface peripheries and optimum hardened oxides. The effect of reducing the pnp base width has been discussed. The tradeoff involved is a reduction of the npn gain. Reduction of the npn base surface area can be achieved by minimizing cell geometry and maximizing the n+ collector areas within the cell. Minimum cell geometry is usually incorporated in I^2L designs for maximum packing density but maximizing the npn collector to base ratio is restrained in LSI arrays to allow for metallization runs between cells and to prevent breakdown or punchthrough between adjacent collectors within a cell.

4.2.3 Transient Ionizing Radiation Hardening

A detailed analysis of the dose rate upset mechanisms in I^2L logic arrays has not been performed. Therefore it is difficult to determine what geometrical and profile variations will maximize the threshold for dose rate upset. Minimum junction photocurrents can be achieved by minimizing the epi thickness, junction areas, and minority carrier diffusion lengths. In the

simplified analysis presented in Section 3, the major variable identified as a possible failure mechanism is the dose rate induced excess positive charge build up in the npn base region which can give rise to a large secondary photocurrent. This excess positive charge can be minimized by using a thin epitaxial region, deep n+ collars or oxide isolation around the inverter cell and a higher doped epitaxy. The tradeoffs involved in these parameters have been discussed. The overriding considerations for maximizing the dose rate upset may well be circuit design and layout. The tradeoffs involved in electrical performance, cell density and power dissipation cannot be anticipated in this analysis.

4.2.4 Electrical Pulsed Overstress Hardening

The small geometries employed in I^2L make the inputs and outputs very susceptible to pulsed electrical overstress. For military applications requiring protection against this environment, some form of T^2L on chip interfacing will probably be required. This will require an isolated form of I^2L with additional chip area to accomodate the T^2L elements as well as additional power drain. The yield may also be affected because of the additional processing steps. If Schottky T^2L buffering is employed in the output the possibility of latchup is also introduced. This will not be a problem with proper design of the interface circuitry. If actual T^2L interfacing is not used then multistage large geometry I^2L buffers will be required. This will also require a larger chip area and power drain but can be achieved with non-isolated I^2L. The use of large geometry buffers will, however, reduce the dose rate upset level.

4.2.5 Summary of Hardness Tradeoffs for First Generation I^2L

The variations in first generation I^2L which should minimize the radiation response are summarized in Table 4.1 by environment. Tradeoffs are listed for each variation.

Table 4.1 Summary of Radiation Hardening Tradeoffs for First Generation I^2L

	Tradeoffs
Neutron Effects	
Minimize npn base width	Lower BV_{CEO}, tighter process control.
Increase npn collector to base area ratio	Lower collector-collector breakdown. Restricted by metallization runs.
Reduce epi thickness	Requires tighter process control. Problem with analog/digital because of linear element breakdown.
Deep n+ collars	Adds process step & increases npn E-B depletion capacitance.
Minimize pnp base width	Decreases npn gain.
Oxide isolation	Possible increase in total dose susceptibility.
Total Dose Effects	
Maximize p region surface doping	Lowers npn BV_{CBO}.
Minimize pnp base width	Decreases npn gain.
Minimize npn base surface area	
Optimize oxide hardness	Increased process control.
Dose Rate Effects	
Minimize epi thickness	See above.
Deep n+ collars	See above.
Oxide isolation	See above.
Increase epi doping	Decreases initial pnp gain.
Pulsed Electrical Overstress	
Schottky T^2L interfaces	Increased power and chip area - possibility of latchup.

4.3 TRADEOFFS FOR RADIATION HARDENED SECOND GENERATION I^2L

The four general categories of second generation I^2L that will be considered for this discussion are ion-implanted, up-diffused, p-epi and substrate fed. All of these approaches represent process variations to the conventional baseline process which could affect circuit design and layout as well as producibility, cost and yield. Whether these effects are adverse or beneficial depends primarily on the company and individuals involved in the design and fabrication of actual LSI circuits. In terms of the number of process steps, none of the above mentioned second generation approaches represent more than one or two additional steps in the formation of a non-isolated basic inverter cell. The processing complexity, at least in terms of the number of required steps, only becomes expanded when the additional complications of isolation, Schottky contacts and clamps, analog/digital combinations, dual level metallization, and input/output interfacing are considered. With the small number of actual I^2L LSI devices on the market, it is very difficult to determine the degree of difficulty in designing and fabricating devices using second generation approaches as well as the impact on producibility yield and cost. From analysis of the radiation effects mechanisms of second generation I^2L, some comments can be made about the important variables and how they will affect performance.

4.3.1 Neutron Hardening Tradeoffs

Most second generation I^2L processes were designed to increase the switching speed over that of the baseline process. This has been accomplished primarily by profile modification of the npn transistor to decrease the emitter-base depletion capacitance and eliminate the retarding electric field in the base. Both of these changes enhance the neutron hardness, either through reduction of the neutron damage coefficient, an increase in initial βu, or both. Therefore, the primary changes which increase performance also increase neutron hardness. This has been experimentally verified on test inverter cells representing three of the four processes where best case minimum prop delays of $\leq$ 10 ns and neutron failure levels of $\geq 10^{14} n/cm^2$ have been demonstrated. The only structure thus far not fabricated for evaluation is the p-epi structure.

Although this preliminary data is encouraging most of it has been taken on optimized test structures (inverter cells and ring oscillators) rather than actual devices, the exception being the T.I. "advanced" (ion-implanted) I^2L ROM.

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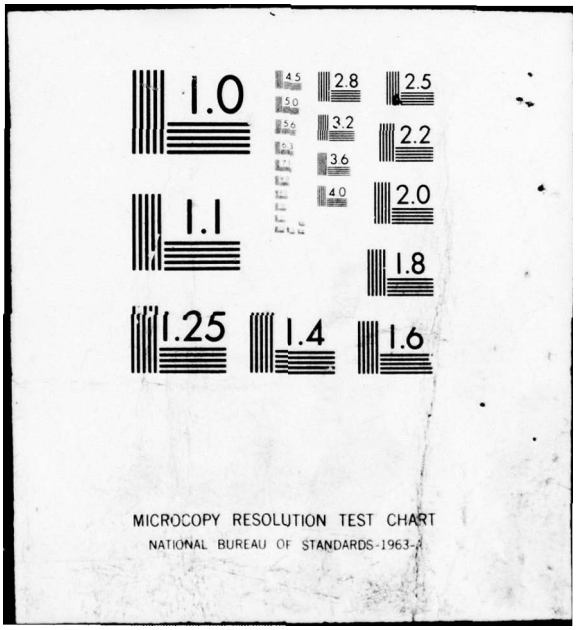
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The performance of actual MSI or LSI devices using the Hughes up-diffused or Harris SFL has not been demonstrated.

The ion-implanted structure represents the least deviation from the baseline process of the four second generation approaches. There are several variations of the ion-implanted process as discussed in Section 2. The increase in neutron hardness of this structure over the baseline structure is due primarily to the intrinsic npn base region. With the T.I. process of ion implantation, the doping profile in the base is reasonably flat thus eliminating the opposing electric field. The doping level in the intrinsic base is also much lower than in the extrinsic base region resulting in a voltage gradient which helps concentrate current flow in the intrinsic region. This would tend to reduce the effect of neutron induced base minority carrier recombination in the extrinsic base region.

The tradeoffs involved in further increasing the neutron hardness of the ion-implanted structure are nearly the same as those for baseline I^2L. Decreasing the lateral pnp base width adversely effects npn gain. Decreasing npn base width can result in unacceptably low collector-to-emitter breakdown voltages. However, with ion implanted bases, better control of the npn base width can be achieved so the design margin is increased. Oxide isolation can reduce lateral hole injection from the npn base but may degrade total dose hardness. Diffusing the p+ injector and npn extrinsic base deeper into the n-epi minimizes the n-epi pnp base volume which will result in higher α values and a smaller pnp damage coefficient. This can only be achieved easily on a relatively thin epi which means tighter process controls.

The up-diffused structure is relatively simple to process and yields very high βu and good neutron tolerance. The nearly inverted doping profile in the npn device yields βu of > 100 with much lower down gains. This could result in current hogging problems if the down gain were much below 20-30. In the Hughes structures, however, down gains are typically greater than 30. This potential problem is also eliminated by the use of Schottky collector contacts and Schottky clamped bases. Use of Schottky collectors also allows for minimum extrinsic npn base volume since the area inside the inverter cell can be one large common collector region with isolation between multiple outputs achieved through the Schottky contacts. This increases βu, reduces the npn damage coefficient and increases speed by reducing the output voltage swing. The tradeoff (as with any Schottky I^2L) is a reduction in on chip noise immunity and

larger photocurrents. The hardening criterion for the lateral pnp transistor is the same as for the baseline structure. Harder pnps could be achieved by using a double diffused structure; however, this would require additional processing steps.

The p-epi structure, first proposed over three years ago, has so far only been used by Fairchild in an Isoplanar form for their 4K dynamic RAM (technically not I^2L). Although little information exists on the difficulties in processing this structure, it is reasonable to assume that there are significant control problems or the structure would have wider use. The structure requires a thin, well controlled epi as well as tightly controlled double diffusion thru the same oxide opening. This represents a significant increase in the processing control and complexity over the baseline structure. Since no neutron effects data has been generated on this structure the potential hardening has not been assessed. Because of the narrow base with graded doping profile the pnp should be much harder than in the baseline structure. The npn transistor neutron hardness will be a function of the epi doping, base width, collector to base area ratio, and isolation technique, the latter two affecting primarily the initial gain. Lowering the p-epi doping will increase the emitter efficiency term but also increase the extrinsic base recombination current and damage coefficient. For a given epi thickness, an optimum doping would have to be determined to maximize both initial βu and hardness. Decreasing the base width will increase both initial and degraded βu but this parameter must be traded off against BV_{CEO} and yield. The narrower the base the greater the control required on epi thickness variations. For a large LSI array this control can be quite critical. The tradeoffs involved for collector to base area ratio and isolation techniques have been discussed for other structures and apply to the p-epi structure.

Substrate Fed Logic (SFL), first announced by Plessey of England, is being investigated by Harris Semiconductor. No other vendor or lab surveyed in this study is working with this structure. Harris chose to work with SFL because of its potential for radiation hardening, its low speed-power product and potentially high speed. Because of the vertical nature of SFL, there is even more interdependency of the pnp and npn transistors than for the other structures. In SFL the pnp active base is not only common to the npn emitter but is the same identical region. This means that changes in the n-epi thickness and

doping level are first order effects for both transistors. Decreasing the n epi thickness will increase pnp gain but decrease npn gain. A primary parameter for emitter efficiency is the ratio of the doping at the p+ substrate to n-epi junction for the pnp transistor and the n-epi to p-epi junction for the npn transistor. Maintaining high ratios improves gain. A suggestion for improving the neutron hardness of this structure is the use of graded doping profiles in the epi regions. This can be accomplished by varying the concentration of the dopant as the epi is grown or by up diffusing the dopant through the epi as it is grown. Grading the epi regions will create an aiding electric field in the base regions which should improve both initial gain and hardness. Grading the epis will, however, make it more difficult to maintain a high ratio of emitter to base doping at the junction which is important for emitter efficiency. Work has begun at Crane to investigate the tradeoffs in neutron hardness versus electrical performance of both the pnp and npn transistors using a one dimensional transistor model.[59] Preliminary analysis has indicated that the constant doped epis presently used by Harris may be harder than proposed graded epis. Graded epis offer greater neutron hardness if high emitter-base junction doping ratios are still maintained; however, this may be difficult to implement. Analysis of the neutron hardening tradeoffs for SFL is still in the early stages, but it is obvious that many tradeoffs are involved. Decreasing the base width of the npn has the same restraints as discussed for the p epi structure.

Most of the geometric and doping profile variables which can be adjusted to increase speed, reduce power and increase βu or fanout also result in increased neutron hardness. This has been verified on three of the four second generation structures. Minimum prop delays of less than 10 ns, minimum speed-power products of less than .5 pJ and fanouts as good or better than for baseline I^2L have been demonstrated on ion-implanted, up-diffused and SFL. This information coupled with neutron test results indicates that electrical performance and neutron hardness are compatible and further increases in performance will lead to even harder parts. While this is true in general, further optimization of the structures for neutron tolerance and electrical performance may involve tradeoffs because of second order effects. This must be addressed through analytical models which include neutron effects. A hardening program should include a modeling effort to optimize the important geometry and doping profiles within the constraints of manufacturability and yield. Such modeling has not yet been performed for neutron effects on second generation I^2L.

4.3.2 Total Dose Hardening Tradeoffs

Of the four second generation I^2L structures discussed in this section, three have been characterized in this study for total dose effects, the ion-implanted structures from T.I., the up-diffused from Hughes and substrate fed from Harris. The three structures reported on in this study all show failure levels well in excess of 10^6rad(Si). The factors which improve total dose response, discussed in Section 3.2, involve minimizing base region surface areas, maximizing p region surface doping, minimizing emitter-base junction surface intersections, and optimizing the oxide. All of these can be achieved without sacrificing performance and many have been employed in second generation I^2L without total dose hardening as a goal.

The T.I. ion-implanted structures have been tested to 10^7rad(Si) without failure above 1 μA/cell operating current. No further improvements would appear to be necessary with this structure. The Harris SFL structures have shown very little change at 10^6rad(Si) and probably will require no further hardening effort for total dose. This structure should have minimal surface effects since the emitter-base junction surface intersection is eliminated in the pnp and minimized in the npn transistor. While the Hughes up-diffused structure has shown reasonably good total dose response further improvement can be made to the lateral pnp structure. One approach would be the use of a double diffused injector such as that used for the p epi device. The tradeoffs involved with the double diffused injector structure were discussed in Section 4.3.1. A less dramatic approach would be optimization of the lateral pnp by going to higher concentration, deeper p+ diffusions and narrowing the base width. This should improve the initial value of α as well as improve the neutron hardness. Minimizing the base width may however adversely effect the npn βu and would reduce processing tolerances. Therefore an optimum value would have to be determined to improve total dose response without adversely effecting βu. Although the results of the total dose response on ITT's up-diffused process have not been reported, an analysis of the structure would indicate several possible problems. Since the p regions are up-diffused all the way to the surface, the surface region is more lightly doped than the region near the substrate. This will cause a concentration of current flow in the base of the lateral pnp near the surface. In addition, the p surface regions have a lower threshold for

depletion and inversion. This will cause severe problems for the npn transistor by increasing emitter-base junction depletion region at the surface. The best solution is to eliminate the up-diffused p region so that it only extends partially through the epi as in the Hughes process. An additional problem with the ITT structure is the use of anodic isolation. Because the isolation oxide has poorer interface properties than the top supface oxide, the positive charge buildup and fast surface state generation can be expected to be larger at this interface. This could lead to problems at the npn emitter-base junction and in the neutral base region of the npn. The total dose response of the ITT structure could be improved by a very shallow p+ implant at the surface of the p regions. In order to minimize the adverse total dose effects of the oxide isolation region, a separate n type diffusion or implantation would be necessary adjacent to the oxide. This would add another processing step which could effect yield and cost and would also reduce packing density.

The use of oxide isolation, such as Isoplanar, V-groove, and anodic, has only been employed by two vendors (Fairchild and ITT) so far, but has been proposed by nearly every vendor for second generation I^2L. The use of oxide isolation decreases side injection, reduces capacitance and improves packing density. In the case of Fairchild's Isoplanar p-epi process, it is used as a diffusion stop for the double diffused lateral pnp.

Total dose problems such as previously discussed for the Fairchild Isoplanar devices can be assumed for other oxide isolated structures. The problem can be significantly reduced by forming an n region next to the oxide. For a structure such as the substrate fed which is built on a p+ substrate, this would have minimum impact since an n region is necessary for contact to the n-epi ground plane. For structures built on an n+ substrate however, the advantages gained in packing density by using oxide isolation would be lost if an n region were diffused next to the oxide wall.

The p-epi process should have excellent total dose hardness of the double diffused pnp. The npn degradation will be primarily a function of the p-epi doping concentration. Increasing the epi doping will reduce total dose effects but will also reduce βu and breakdown voltages. Therefore, an optimum value of epi doping will have to be determined to maximize total dose response while maintaining performance.

With the exception of the oxide isolation problem there appears to be little reason for concern about the total dose response of second generation I^2L. Failure levels of greater than 10^6rad(Si) appear to be achievable without sacrifices in performance, yield or cost.

4.3.3 Transient Ionizing Radiation Hardening Tradeoffs

The tradeoffs involved in dose rate hardening of second generation I^2L are difficult to assess. First, there have been no dose rate upset tests performed on second generation test structures or devices. Second, there have been no analytical models developed to evaluate dose rate upset mechanisms in I^2L, either baseline or second generation. In the simplified analysis presented in Section 3.3, the main parameter identified as affecting dose rate response is the hole density in the base, which can turn the npn transistor on (if it is off) and lead to a secondary photocurrent. For a large LSI array, however, the first order effect may be the unbalance between opposing photocurrents that determines upset. If this is the case cell design and geometry as well as circuit layout may have to be optimized to increase dose rate upset levels. The impact of this on performance, yield and cost cannot be determined at this time.

A first approach for the dose rate environment would be minimization of inverter cell photocurrents. This can be achieved by minimizing cell geometries (especially the npn base area) and minimizing the minority carrier diffusion length in the n regions (npn collector and emitter area). Although minimizing the npn base area is compatible with increasing βu and speed, altering the n region doping to minimize the minority carrier diffusion length may cause several tradeoffs in performance. Increasing the n-epi doping level will decrease initial pnp gain although it would probably increase initial npn gain. This same tradeoff is involved in optimizing the neutron hardness of the pnp.

Secondary photocurrents involve an amplification of the ionization induced excess base current by the βu of the npn. Devices having very high up gains, such as the up-diffused devices would experience greater problems with secondary photocurrents than with other structures. Reducing the βu however, would decrease the neutron failure level unless appropriate measures were taken to optimize the neutron damage coefficient.

For an npn transistor in the on state, the excess base charge will increase the operating current. If the devices are being operated near peak βu, this increase in operating current might drive the transistor to the point

at which the βu drops below one, causing the transistor to come out of saturation. This would be most critical for the outputs farthest from the base current source. This problem can be reduced by increasing the current at which peak βu occurs and minimizing the high-current gain fall off. This is normally achieved by going to larger geometries and reducing the lateral base resistance. Going to larger geometries is not recommended since this would mean a reduction in packing density, speed, and neutron hardness. The lateral base resistance can be reduced by going to a wider or more heavily doped base. A wider base would reduce gain, speed and neutron hardness and higher doping in the base could reduce gain by reducing the emitter-base voltage drop in the intrinsic base region.

A possible way to reduce the problem without affecting performance would be to minimize the distance from the base contact to each of the collector outputs within the inverter cell. This can be done by limiting the number of outputs per cell, placing the base contact in the center of the cell and/or changing the cell geometry from single row of outputs to one having two rows. Such arrangments would not adversely effect electrical performance but would affect cell layout and packing density.

4.3.4 Electrical Pulse Overstress Hardening Tradeoffs

Since the electrical pulse overstress problem in I^2L is limited primarily to inputs and outputs, the same tradeoffs which were discussed for baseline I^2L in Section 4.2.4 apply to second generation I^2L. The major question for second generation structures will be how easily the on chip T^2L interfaces can be implemented.

A possiblity for future military applications of I^2L is the concept of total I^2L modules. If, for instance, a complete family of I^2L computer chips were available, a processor module could be built from non-buffered I^2L devices. The module itself could be T^2L interfaced with a separate chip containing all the necessary buffering. Such a system would eliminate the need for on chip T^2L interfacing resulting in greater packing density and lower power dissipation. Electrical pulse overstress should not be a problem for total I^2L packages since the devices themselves should not generate photocurrents of sufficient magnitude to cause junction or metallization burnout.

4.3.5 Summary of Radiation Hardening Tradeoffs For Second Generation I^2L

Various forms of second generation I^2L have been introduced in the past few years, primarily to increase speed over that achieved with baseline I^2L. Although none of the advanced structures were designed specifically to address radiation hardening, the resulting changes employed to increase speed have generally resulted in better radiation performance. There are few if any "tradeoffs" involved, since the goal of second generation structures is performance; and increased radiation hardness comes as a side benefit. The one exception is the total dose response of Isoplanar structures. In this case the hardness is reportedly not as good as for baseline structures. Since no data has been reported on the neutron response of the Fairchild or ITT structures it cannot be verified that all higher speed second generation devices will be harder. However, it seems reasonable from the analysis that the neutron response should be improved.

Even though increased performance has yielded, for the most part, increased hardness, several additional changes have been suggested to further increase the hardness of second generation I^2L. These are summarized in Table 4.2 along with the tradeoffs involved.

Table 4.2 Summary of Radiation Hardening Tradeoffs For Second Generation I^2L

Proposed Changes To Increase Radiation Hardness.			Tradeoffs Involved.
Environment	Structure	Changes.	
Neutrons	Ion-Implanted	Same as for baseline I^2L.	Same as for baseline I^2L.
	Up-diffused	Use of double diffused pnp structure.	Increased processing and lower yields.
	p-epi	Minimize epi thickness.	Process control and yield.
		Maximize collector area.	Increases possibility of shorting collectors.
		Minimize npn base width.	Process controls on epi uniformity.
	SFL	Use of graded epis.	Increased processing complexity.
		Minimize npn base width and epi thickness.	Same as for p epi process.
Total Dose	Ion-Implanted	Utilize deep heavily doped p diffusions and narrow pnp base width as with T.I. structure.	None
	Up-diffused.	Double diffused injector or optimize conventional lateral pnp.	Additional process complexity and possible yield loss for double diffused injector.
		Utilize up-diffusion as in Hughes structure rather than up-diffusing completely through epi.	None
	p-epi	Maximize epi doping concentration.	Npn gain and breakdown voltage limitations.
	SFL	None	
	Oxide Isolated	n diffusion or heavily doped p adjacent to isolation	Additional process step. Reduced speed and packing density.
Dose Rate	All	Minimize junction areas.	None
		Maximize n region doping.	Reduces pnp α and neutron tolerance.
		Minimize distance between outputs and input.	Restriction on cell design and layout.
Electrical Pulse Overstress	All	Same as for baseline I^2L.	

SECTION 5

COMPARISON OF I^2L TO OTHER LSI TECHNOLOGIES

The use of I^2L in hardened military system applications will depend on its performance advantages/disadvantages as well as its radiation hardening capabilities. Therefore, in order to determine the potential usefulness of I^2L military LSI applications, a study was performed by Mission Research Corporation - San Diego to compare I^2L to other developing bipolar and MOS LSI technologies.[53] The bipolar technologies considered are:

1. TTL
2. Schottky-clamped TTL (S/C TTL)
3. Radiation-hardened TTL (R/H TTL)
4. Emitter coupled logic (ECL)

The MOS technologies considered are:

1. p-MOS
2. n-MOS
3. Bulk CMOS (Aluminum gate)
4. CMOS/SOS (Aluminum gate)

The parameters considered as a basis of comparison are:

1. Cell density
2. Switching speed
3. Power dissipation
4. Speed-power product
5. Output drive capability
6. Noise immunity
7. Operating temperature range
8. Power supply requirements
9. Processing complexity

Comparison of evolving LSI technologies is difficult because of the wide variations in the nature of competing technologies and the variety in requirements of potential applications. Considering I^2L in particular, there is little information on standard products for direct comparison in general applications.

Results of comparing I^2L performance to other LSI technologies are summarized subjectively in Table 5.1. These results are supported by quantitative analysis as presented in the remainder of Section 5. From this subjective comparison, it is clear that I^2L is a superior LSI technology in terms of cell density, power dissipation and speed-power product. I^2L is better in switching speed, output drive capability and temperature range than most MOS technologies, but is generally weaker than most bipolar technologies in these categories. On the other hand, I^2L is at a definite disadvantage to both bipolar and MOS technologies in terms of noise immunity. All of the microcircuit technologies are capable of performance over the full military operating temperature range (-55 to +125°C) with the exception of n-MOS, which is generally restricted to 0 to 70°C operation. In general, the temperature design problems are most critical for bipolar technologies at low temperatures and most critical for MOS technologies at high temperatures.

5.1 CELL DENSITY

Cell density is a critical LSI parameter which reflects component yield. For a wafer with spacially-distributed defects, increasing cell density can allow arrays of given complexity to be realized at greater yield.

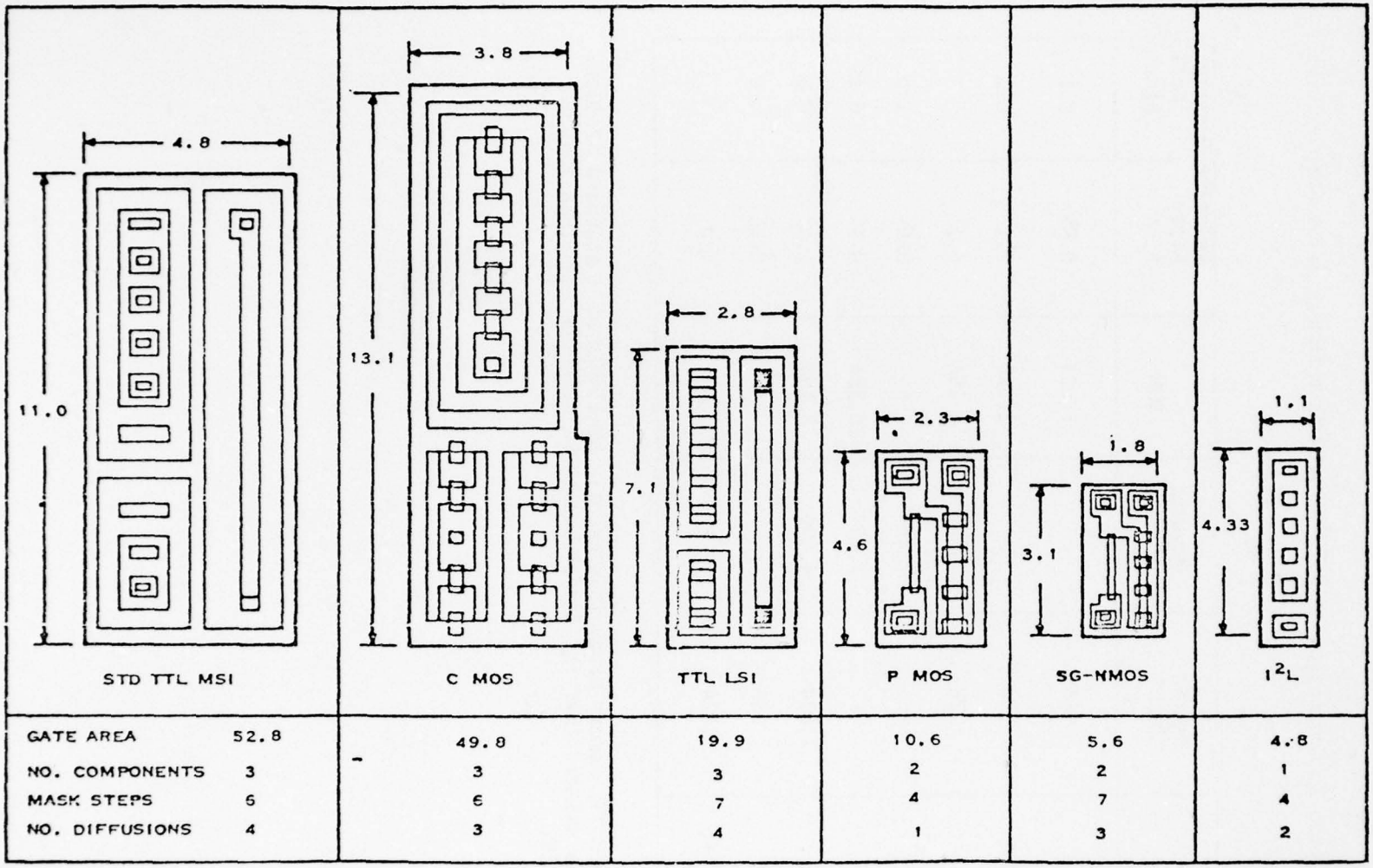
Two criteria can be considered as representative of cell density for a given LSI technology. The first is the geometry of a basic logic cell for state-of-the-art mask-layout rules. Typically this would be a basic inverter of nominal fan-out capability. A second criterion representative of cell density is the maximum complexity of available arrays. This has the advantage that practical limitations due to layout problems and overall processing complexities are implicitly included. The disadvantage of using maximum complexity of arrays as a criteria is the difficulty in defining an accurate measurement of element complexity for arrays of different functions and technology. As a practical matter, then, the comparison must be made of memory arrays of common function which gives a subtle advantage to those technologies that lend themselves to a larger number of regular, simple cells. This, then, may not be completely representative of combinational LSI logic arrays.

Logic cell geometries for several of the LSI technologies which are defined in Figure 5.1[15] are representative of the logic cell criteria. Typical memory array complexities presently available are summarized in Table 5.2 as

Table 5.1 Subjective Comparison Of LSI Technologies

	TTL	S/CTTL	R/HTTL	ECL	IIL	PMOS	nMOS	CMOS	CMOS/SOS
cell density	-	0	--	-	++	+	++	0	++
switching speed	0	+	+	++	0	-	0	-	++
static power dissipation	-	-	-	--	+	0	+	++	++
dynamic power dissipation	+	+	+	+	++	0	+	0	+
speed-power product	-	0	-	0	++	0	+	0	++
output drive capability	++	+	+	+	+	-	0	-	--
noise immunity	+	+	+	0	--	0	0	++	++
temperature range	+	+	+	+	+	0	-	0	-

++ superior, + good, 0 average, - below average, -- weak



GATE AREA	52.8	49.8	19.9	10.6	5.6	4.8
NO. COMPONENTS	3	3	3	2	2	1
MASK STEPS	6	6	7	4	7	4
NO. DIFFUSIONS	4	3	4	1	3	2

Figure 5.1 Representative Logic Cell Geometries[15]

Table 5.2 Comparison of Cell Density from Memory Array Complexities

	Static RAM	Dynamic RAM	ROM	Relative Density	
				Array Size	Cell Size
TTL	64	-	1.024	0.05	0.1
S/C TTL	256	-	2,048	0.2	0.2
ECL	128	-	256	0.1	-
I^2L	-	4,096	-	1.0	1.0
p-MOS	-	1,024	16,384	0.5	0.45
n-MOS	1,024	4,096	8,196	1.0	0.8
CMOS	256	-	-	0.25	0.1
CMOS/SOS	1,024	-	-	1.0	-

*No R/H TTL memory array is presently available as a standard product. It is assumed that the density would be slightly less than that of S/C TTL.

representative of the alternate criterion. Even for the memories, however, there are variations in coding and decoding, as well as variations in yield that are considered acceptable at a marketplace price.

Considering these criteria, it seems reasonable to state that I^2L offers the highest cell density of all bipolar technologies, and that it is comparable to that of silicon-gate n-MOS and CMOS/SOS which are comparable as the highest cell density of the MOS technologies. Specific variations between I^2L, n-MOS, and CMOS/SOS will depend principally on the cleverness of the design, allowable design margins in circuit and processing parameters, and the severity of environmental requirements. It is interesting to note that each of these high-density technologies are based on commercial products, and each, in turn, are highly susceptible to radiation effects.

For other bipolar technologies, it appears that low power Schottky-clamped TTL is of highest cell density with a slight edge over ECL, conventional TTL and radiation-hardened TTL. The principal reason that these bipolar technologies are an order-of-magnitude less dense than I^2L is the area required by diffused or thin-film resistor elements. This is compounded in overall performance considerations by the increase in resistor geometry generally necessary in low-power designs making both objectives in contrast.

Improved cell densities in MOS technologies are the result of replacing load resistors by small-geometry active elements. In addition, CMOS/SOS elements can be closed-spaced on a dielectric substrate. The advantage of silicon-gate n-MOS is the exclusive use of high mobility n-MOS transistor elements and an effective two-layer cell interconnection capability. The relative decrease in density for p-MOS is due to the relatively low channel mobility. The cell density of bulk CMOS is limited by the relatively large number of elements required as well as the necessity of guard bands to prevent parasitic transistor effects. In general, however, all MOS technologies offer a substantial advantage in cell density compared to bipolar technology with the recent exception of I^2L. This advantage in cell density has been a major factor in the rapid development of MOS/LSI.

5.2 ELECTRICAL SWITCHING SPEED

The electrical switching speed of an array is determined by the signal propagation delay of the internal logic cells and by the time required to

Table 5.3 .Summary of LSI Switching Response

Technology	Propagation Delay	Load	Test Conditions
a. TTL: 54L	33 ns	50 pF/4KΩ	V_{cc} = 5 V
TTL: 54	10 ns	15 pF/400Ω	V_{cc} = 5 V
TTL: 54H	6 ns	25 pF/280Ω	V_{cc} = 5 V
S/C TTL: 54LS	10 ns	15 pF/2KΩ	V_{cc} = 5 V
S/C TTL: 54S	3 ns	15 pF/280KΩ	V_{cc} = 5 V
R/H TTL: R54L	45 ns	50 pF/4KΩ	V_{cc} = 5 V
R/H TTL: R54	10 ns	15 pF/400Ω	V_{cc} = 5 V
R/H TTL: R54H	8 ns	25 pF/280Ω	V_{cc} = 5 V
ECL	2 ns		V_{EE} = -5.2 V
I^2L	1 μs	C_L = 10 pF	I_{EE} = 1 μA
I^2L	20 ns	C_L = 10 pF	I_{EE} = 50 μA
I^2L	10 ns	C_L = 10 pF	I_{EE} = 1 mA
b. p-MOS	250 ns	C_L = 20 pF	+5 V/-12 V
n-MOS	100 ns		
c. CMOS	70 ns	C_L = 20 pF	V_{DD} = 5 V
CMOS	30 ns	C_L = 20 pF	V_{DD} = 10 V
CMOS	25 ns	C_L = 20 pF	V_{DD} = 15 V
d. CMOS/SOS	2 ns	ring counter	V_{DD} = 10 V
CD4007	4 ns	C_L = 2.8 pF	V_{DD} = 12 V
CD4007	25 ns	C_L - 20 pF	V_{DD} = 10 V

a. T. I. TTL Data Book for Design Engineers
b. T.I. MOS/LSI Standard Products Catalog
c. RCA COS/MOS Data Book
d. NRCT CMOS System Study Report

drive an external load. In addition, the nature of switching speed, as influenced by operating conditions, varies between LSI technologies. This variation with test condition can be defined into three categories:

1. Fixed supply voltage, switching response such as TTL, S/C TTL, ECL, p-MOS, n-MOS.
2. Variation of switching time with supply voltage such as CMOS, and CMOS/SOS.
3. Variation of switching time with bias current such as I^2L

where there is a variation in each case with specified load.

Typical switching times (i.e., propagation delay) are summarized in Table 5.3 for the variety of LSI technologies. For the TTL technologies the switching time varies with the design parameters as reflected by the nominal, -L and -H standard series. Similarly, the switching response of ECL arrays is a function of circuit design. The value quoted in Table 5.3 is representative of the Motorola 10,000 series which is a compromise between the fastest switching speed and power dissipation.

Electrical switching response of MOS/LSI arrays is a function of design for single-polarity (p- or n-MOS) or design and supply voltage for CMOS. In general, the switching time decreases with increasing supply voltage, but the nature of the circuit operation requires specific voltages for p-/n-MOS, but CMOS can be operated over a wide range in supply voltage. Increasing the supply voltage also increases the output drive capability of a CMOS array. The supply voltage is limited, however, by drain-source punch through of individual transistor elements.

Electrical switching response of I^2L is a function of the injector bias current. At low currents the speed-power product is constant. Therefore, 1 pJ I^2L will have a propagation delay of approximately 200ns at a bias current of 1 μA per stage. At high bias currents, the switching response is limited by carrier storage time in the npn transistor element. The minimum propagation delay is on the order of 10 ns for first generation I^2L technology.

From the data presented in Table 5.3, it appears that bipolar technology generally has a switching speed advantage over the MOS technology. The overlapped exceptions are I^2L which is a relatively slow bipolar technology, and CMOS/SOS which is the fastest of the MOS technologies.

5.3 POWER DISSIPATION

The power dissipation in an LSI array is to various degrees a function of cell design, clock rate (or frequency of operation) and output loading. For bipolar technologies the power dissipation is generally the same for either static or dynamic operation and determined by either the fixed circuit design or bias current. For p-/n-MOS technology, the power dissipation increases with increasing frequency of operation, but the static power dissipation (exluding dynamic-only arrays) is a significant fraction of the total. CMOS arrays, on the other hand, exhibit very low static power dissipation, but a strong variation of dynamic dissipation with frequency of operation and output load.

Logic cell power dissipation for the LSI technologies are summarized in Table 3.4 for static operation and operation at a clock rate of 1 MHz.

In general, the MOS technologies have an advantage in power dissipation over the bipolar technologies, with the dramatic exception of I^2L. The low power dissipation of I^2L and CMOS at low clock rates is particularly impressive. The principal difference is, however, that the low power operation of I^2L must be obtained by low bias and long switching times must be specified, while with CMOS, the switching transistor time remains constant, but the total average power dissipation decreases with decreasing clock frequency.

5.4 SPEED-POWER PRODUCT

Because of the complexities in comparing switching speed and power dissipation between various LSI technologies, the product of power dissipation and switching speed has been used as a figure of merit. For most LSI technologies, this is a straightforward product of the static power dissipation and logic cell propagation delay.

The calculation becomes more complex, however, when the dynamic power dissipation dominates the static power dissipation. An additional question, common to all new low-power LSI devices, is accounting for the energy which must be committed to the external capacitive load. For a logic swing of 5 volts and a 20 pF output capacitance, the load energy is 250 pJ. This is a very significant energy in an LSI technology where the internal energy for information storage is comparable to or less than the load energy.

Speed-power products for the LSI technologies are summarized in Table 5.5.

Table 5.4 Summary of LSI Power Dissipation

	Power Dissipation Per Gate		Test Conditions
	Static	Dynamic	
TTL: 54L	1 mW		V_{CC} = 5 V
54	10 mW		V_{CC} = 5 V
54H	22 mW		V_{CC} = 5 V
S/C TTL: 54LS	2 mW		V_{CC} = 5 V
54S	19 mW		V_{CC} = 5 V
R/H TTL: R54L	1 mW		V_{CC} = 5 V
R54	10 mW		V_{CC} = 5 V
R54H	23 mW		V_{CC} = 5 V
ECL	25 mW		V_{EE} = -5.2 V
I^2L	0.7 μW		I_{EE} = 1 μA
	40 μW		I_{EE} = 50 μA
	800 μW		I_{EE} = 1 mA
p-MOS	1 mW		
n-MOS	0.3 mW		Intel 2104
CMOS (CD4000B)	5 μW	1.5 μW/kHz	V_{DD} = 5 V
	10 μW	6 μW/kHz	V_{DD} = 10 V
	15 μW	16 μW/kHz	V_{DD} = 15 V
CMOS/SOS	12 μW	15 μW/kHz	V_{DD} = 12 V

5.5 OUTPUT DRIVE

Consideration of output drive and comparison of LSI is another complex situation. In general, either MOS or bipolar elements can be designed to virtually any microelectronic load. The practical restriction, however, is the total element geometry that can be committed to the output interface necessary. In MOS technologies, the output drain current of a transistor element can be expressed up to pinch-off as,

$$I_D = \frac{\mu\varepsilon_{ox}}{2t_{ox}} \cdot \frac{W}{L} \quad 2(V_{gs} - V_t)V_{ds} - V_{ds}^2$$

With the minimum length of the channel restricted by mask tolerances with considerations of voltage breakdown, the output conductance is then proportional to the channel width. Increasing the channel width, however, increases the gate capacitance of the output stage and increases the capacitance load on the internal logic cell. This increase in capacitance has a first-order effect on cell electrical switching response time.

The output conductance of a MOS transistor element is proportional to the channel mobility. Thus, n-channel elements have an advantage of about a factor-of-three over p-channel elements due to the relative values of electron and hole mobilities in bulk silicon. The decrease in carrier mobility with increasing temperature is a significant design consideration for MOS arrays.

The output conductance of MOS elements on sapphire is somewhat less than that of bulk silicon due to a decrease in carrier mobility. This decrease in mobility may be as great as a factor-of-three for thin silicon films on a sapphire wafer. Research is still under way to improve the semiconductor quality of the silicon film.

For bipolar transistors, the output drive is typically that of a common-emitter collector current which is proportional to the area of the transistor within limits of sustaining current gain at the required current density and limitations of current crowding and high-level injection.

In general, for elements of comparable geometry, the output drive capability of bipolar elements is substantially greater than that of MOS elements.

Table 5.5 Summary of LSI Speed-Power Products

TTL:	54L	33 pJ	V_{CC} = 5 V
	54	100 pJ	V_{CC} = 5 V
	54HH	132 pJ	V_{CC} = 5 V
S/C TTL:	54LS	19 pJ	V_{CC} = 5 V
	54S	57 pJ	V_{CC} = 5 V
R/H TTL:	R54L	45 pJ	V_{CC} = 5 V
	R54	100 pJ	V_{CC} = 5 V
	R54H	173 pJ	V_{CC} = 5 V
ECL		50 pJ	V_{EE} = -5.2 V
I^2L		0.5 pJ	I_{EE} = 1 μA
		1.0 pJ	I_{EE} = 50 μA
		5.0 pJ	I_{EE} = 1 mA
p-MOS		100 pJ	
n-MOS		10 pJ	
CMOS*		125 pJ	V_{DD} = 5 V, C_L = 0
		500 pJ	V_{DD} = 10 V, C_L = 0
		2400 pJ	V_{DD} = 15 V, C_L = 0
		750 pJ	V_{DD} = 5 V, C_L = 50 pF
		3000 pJ	V_{DD} = 10 V, C_L = 50 pF
		8000 pJ	V_{DD} = 15 V, C_L = 50 pF
CMOS/SOS*		72000 pJ	V_{DD} = 12 V

*Energy per switching transition

Of the bipolar technologies, I^2L is at a principal disadvantage because of the relatively low gain of the output inverter. Alternative output networks have been suggested which take advantage of high transistor gain, but may involve isolation techniques that may introduce the possibility of latch-up. Also, as opposed to MOS technologies, the worst-case for bipolar elements is at low temperature where transistor gain is minimum.

For MOS technologies, n-MOS is most favorable for output conductance and CMOS/SOS the least favorable.

5.6 NOISE IMMUNITY

Noise immunity is one of the most complex parameters to define for any technology, as well as difficult to compare between technologies. It can be defined in a variety of ways and should be referenced to both the input terminal of a logic cell as well as to the power supply.

Referred to the input, the performance measure is the voltage, current, and/or energy required to induce a logic error with the logic element at the most sensitive bias of the 0- or 1-logic state. A similar definition can also be used at the power-supply terminal and should also (but almost never) be considered. That is, in a technology such as TTL, and CMOS, there is a significant power supply current transient during switching. The requirement for voltage regulation must then be consistent with power supply filtering to minimize the effects of the signal-induced current surges. It is suggested that for LSI arrays, power supply/ground noise immunity is more critical than input noise immunity. Just as for output conductance, it is necessary to specially design the interface cells of an array, even with trade-offs in element geometry and power dissipation. Generally, interface networks for both n-MOS and I^2L are designed to be essentially those of TTL and it is expected that interface noise immunity would be comparable. Power supply/ ground noise immunity, however, is common to all internal logic cells of the LSI array.

In terms of voltage noise margin, as summarized in Table 5.6, CMOS (either bulk or SOS), with a noise margin approximately equal to 45 percent of V_{DD}, has a clear advantage over other bipolar and MOS technologies. The noise margins of n-MOS are essentially the same as that of TTL-compatible interfaces. For bipolar technologies, the voltage noise margin of ECL is

somewhat less than that of TTL. There is no published experimental data on the interfaced voltage noise margins of I^2L. Calculated results[58] indicate the worst-case noise margin as approximately 60mV, which is significantly less than TTL and substantially less than CMOS.

An analytical and experimental investigation of the noise characteristics of I^2L was conducted to more fully define the DC and AC noise immunity. The total logic swing of an I^2L gate (LS) is made up of the "off" noise margin (NM_{off}), the transistion region (TR) and the "on" noise margin (NM_{on}) as shown in Figure 5.2.

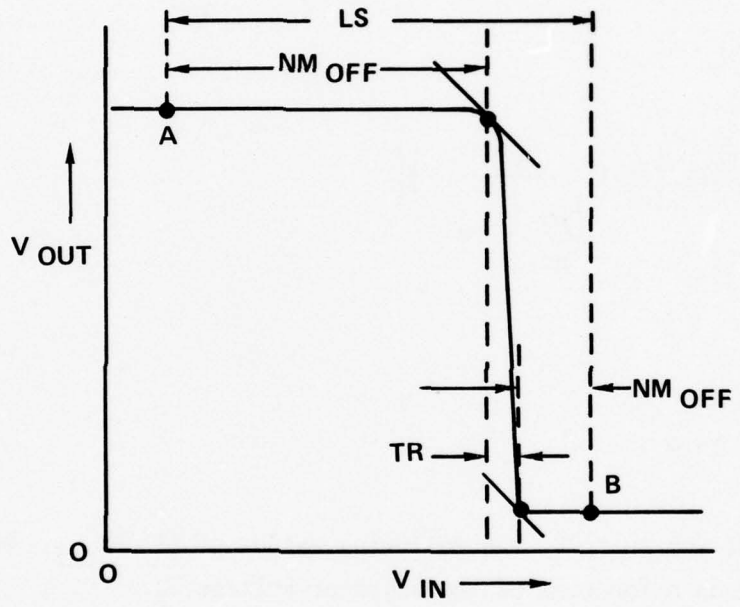


Figure 5.2 Definition of "On" and "Off" Noise Margin, Logic Swing, and Transition Region

The transition region is defined as the difference in voltage between the two unity gain points of the V_{out} vs. V_{in} curve.

Using the definitions of I_{po}, I_{no} (base-emitter saturation currents of pnp and npn, respectively) and βn given in Ref. 58 the following analytical expressions were derived.

$$LS = V_B - \frac{kT}{q} \left\{ \ln \left(1 + \frac{1}{\frac{I_{po}}{I_{no}} \beta n} \right) + \frac{I_{po}}{I_{no}} + \beta n^{-1} \right\}$$

$$NM_{off} = V_B - \frac{kT}{q} \left\{ \ln \left(\frac{2I_{no}}{I_{po}} \right) + \frac{I_{po}}{I_{no}} + \beta n^{-1} \right\}$$

$$NM_{on} = \frac{RT}{q} \ln \left\{ \tfrac{1}{2} \left(\frac{1}{\frac{I_{po}}{I_{no}} + \beta n^{-1}} \right) \right\}$$

$$TR = \frac{kT}{q} \ln 4$$

Assuming $\frac{I_{po}}{I_{no}} = 0.05$ and $\beta n = 20$, the following values of LS, NM_{off}, NM_{on} and TR were calculated as a function of the injector voltage V_B.

	V_B		
	600 mV	800 mV	1.0V
LS	579.3mV	779.3mV	979.3mV
NM_{off}	501.5	701.5	901.5
NM_{on}	41.8	41.8	41.8
TR	36.0	36.0	36.0

From these calculations it can be inferred that (a) the "on" and "off" voltage noise margins of I^2L are extremely skewed compared to T^2L and CMOS and (b) the "on" noise margin and transition region are invarient to the injector voltage.

Measurements of the AC noise immunity characteristics of RCA I^2L inverters were made to determine the input noise voltage and current required to cause a change of state as a function of the pulse width. The square wave input signal was applied with a pulse generator and the change of state was sensed with an I^2L flip flop as described by RCA for their CMOS noise immunity measurements (COS/MOS Digital Integrated Circuit Databook, 1974, pages 386 and 387). An attempt was made to measure the input current of the noise signal with a current probe. However the sensitivity of the probe was not adequate to accurately determine the current amplitude. The results of "on" voltage noise immunity measurements agreed quite well with the calculated results. For pulse widths greater than 400ns, NM_{on} was 57mV (V_B = 800mV). Below 400nSec the noise immunity increased as expected. For a 200ns pulse width, NM_{on} was 90mV, at 100ns, 135mV and at 50ns, 280mV. In the "off" state the noise immunity was constant at 720mV above 600ns (V_B = 800mV). However, for the narrower pulse widths ($\leq$ 400 ns), NM_{off} reached a constant value of 775mV rather than increasing with decreasing pulse widths as expected. No further investigation has been conducted to explore the reason for this result.

Noise immunity considerations at the power supply terminal should include both the range of voltage or current which can be accommodated and the regulation requirements resulting from current or voltage pulses. In this case, TTL, ECL, p-MOS and n-MOS arrays require well regulated supply voltages (total variation less than one volt). This is a significant requirement for TTL because of the power supply current surges that occur during a switching transient. On the other hand, both CMOS and I^2L have a high tolerance for variations in power supply voltage or current. In CMOS, a decrease in supply voltage results in a decrease in switching speed and noise margin but does not result in operational failure. Typically the CMOS supply voltage can be selected from 5 to 15 V. In an I^2L array, operation is credible over a wide range of power supply bias currents (typically 1 μA to 1 mA per gate). As the power supply current is decreased, however, the electrical switching time is increased.

Table 5.6 Noise Immunity Summary

Logic Family	D-C Bias	D-C Noise Margin V_{NL}	D-C Noise Margin V_{HL}	Minimum Noise Energy E_{NL}	Minimum Noise Energy E_{HL}
TTL	5 V	1.2 V	2.2 V	1.7 nJ	1.0 nJ
CMOS	5 V	2.2 V	2.2 V	1.0 nJ	0.9 nJ
(bulk)	10 V	4.5 V	4.5 V	3.7 nJ	3.1 nJ
	15 V	6.8 V	6.8 V	7.2 nJ	8.5 nJ
I^2L	1 μA	0.6 V	0.06 V	25 nJ	0.3 pJ
	50 μA	0.65 V	0.06 V	0.72 nJ	0.6 pJ
	1 mA	0.75 V	0.06 V	0.49 nJ	5 pJ

Noise immunity at signal interfaces can also be characterized in terms of the noise energy required to cause a logic error rather than the noise voltage level. This noise energy can be defined as

$$E_N = V_N \cdot I_N \cdot t_p$$

where V_N and I_N are the noise voltage and current for a given pulse width, t_p, at the interface node as shown in Figure 5.3.

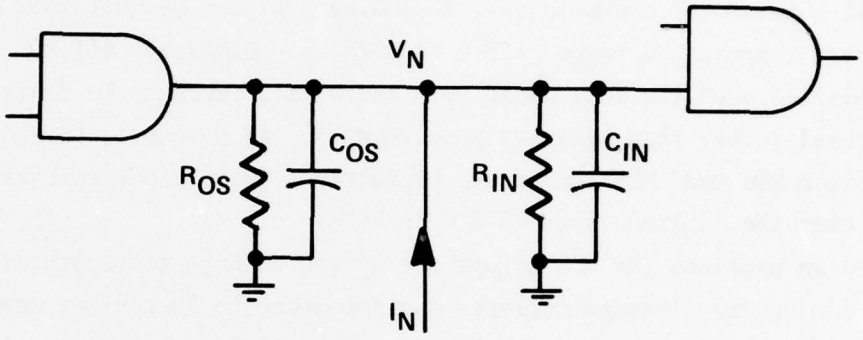


Figure 5.3 Gate Noise Immunity Characterization

The driving point impedance at the interface node is essentially the parallel combination of the resistances and the sum of the non-linear capacitances. If the conductances are large compared to the capacitive susceptances, the expression for noise energy can be approximated as

$$E_N = \frac{V_N^2}{R_o} \cdot t_p$$

where R_o is the combined driving-point resistance. Calculations in a Motorola application note using the resistive form of the energy equation are shown for TTL and CMOS technologies in Table 5.6. Corresponding calculated values for I^2L are shown and are based on a 1 pJ speed-power product technology.

Considered in terms of noise energy, the critical energy is approximately that committed to the storage of digital information in an array, which is reflected by the speed-power product of a technology. It is clear that a low-power technology will tend to low noise immunity, and input and output interfaces must be transformed to high energy levels (such as TTL or CMOS). This has been the case in the evolution of silicon-gate n-MOS memories where internal noise margins are less than 200 mV, but input/output interfaces are at TTL levels.

5.7 TEMPERATURE RANGE

All bipolar LSI technologies, including I^2L, can be qualified over the full military temperature range (-55^oC to $+125^oC$). Similarly all MOS technologies can be qualified over the full range, but there is a tendency to design MOS/LSI for commercial rather than military requirements. As a result, virtually all silicon-gate n-MOS and CMOS/SOS arrays presently available are specified for operation over the limited range of 0^oC to 70^oC.

Design problems for MOS arrays are severe at high temperatures due to increases in junction leakage currents and the decrease in carrier mobility. Conversely, the design problems for bipolar technologies are most severe at low temperatures because of the decrease in transistor gain.

5.8 POWER SUPPLY REQUIREMENTS

All I^2L logic arrays operate from the injector current which is supplied by forward biasing the emitter to base junction of the pnp injector transistor. The current voltage relationship for this forward biased junction follows the simple diode relationship

$$I_{INJ} = I_S \exp\left(\frac{qV_{BE}}{kT}\right)$$

where V_{BE} is junction voltage drop. For large logic arrays the total injector current may reach 100-300 mA (assuming 1000-3000 gates operating at 100 μA/gate for maximum speed). At 100 μA/gate the V_{BE} will be approximately 700 mV, thus a single 1V, 1A power supply will be adequate for any I^2L device. However, many I^2L devices are presently interfaced with T^2L or ECL buffers.

Therefore, in the practical sense, the power supply requirements for I^2L LSI devices will be the same as that required for the interfacing since the I^2L logic can be operated from any positive supply voltage greater than 1V. The I^2L products announced by Fairchild and Signetics require a single 5V supply. T.I. on the other hand, has so far used open collector I^2L interfacing which requires a single 1V supply for the I^2L device but an additional 5V supply for external pull-up if used with T^2L. With ECL interfacing a +1V and a -5.2V supply are required. In the case of circuits using an analog/digital mix the supply requirements will be those for the analog portion, generally +15V and -15V. Although power supply requirements for bipolar devices are rather simple and consistent, the requirements for MOS devices vary considerably from single (+5 to +15V) supplies for static NMOS and CMOS to three supplies (+5, -5 and +12V) for dynamic n-MOS. Because of the large variations in power supply requirements depending on the circuit functions, there is no clear advantage of one technology over another. If I^2L is to be used directly with other I^2L circuits with no on-chip buffering, then well regulated 1V power supplies need to be developed to minimize power dissipation.

5.9 PROCESSING COMPLEXITY, YIELD AND COST

At this point in time any discussion of high density LSI processing and yield comparisons between various technologies is speculative. The highest density technologies are n-MOS, I^2L and CMOS/SOS. Of these only n-MOS has an appreciable number of the LSI devices in production. An extensive discussion of the status of I^2L LSI parts was given in Section 2. Only 5 devices are commercially available. There is only one vendor of commercial LSI level CMOS/SOS, RCA. RCA has one device in production that is commercially available (1K static RAM) and it is not presently being built on a commercial production line. Hewlett-Packard is producing several aluminum gate CMOS/SOS LSI devices for use in their calculator line, but these circuits are not available commercially. Without the commercial production base it is most difficult to determine cost and yield comparisons. Yield is a function of the types and quality of the materials used, the number and complexity of the individual processing steps, and certainly in the case of MOS, the cleanliness of the processing. Cost, while certainly a function of yield, is also a function of packaging, testing, and market. The only factors which affect yield and cost that may reasonably be projected at this time, based primarily on laboratory

data, are processing complexity and the purity and cost of materials. CMOS/SOS requires very high purity sapphire substrates. The cost of sapphire substrates is much higher than silicon substrates (3 inch wafers cost $30-$80 versus $4-$5 for silicon).[55] The purity of the sapphire substrates also affects static power dissipation. Efforts are under way to improve purity and lower cost but at the present these factors mean much higher cost for CMOS/SOS. n-MOS devices are relatively easy to process and have high yields and low cost. However, they cannot be used in military systems having a total dose requirement. Data has shown[56] that n-MOS dynamic RAMs fail at a few thousand rads (Si). The processing complexity, yield and cost of I^2L is more difficult to evaluate than either n-MOS or CMOS/SOS. There is no single "commercial" I^2L process. Since many second generation approaches have been taken to I^2L to improve performance, there are now several different structures with varying degrees of processing complexity being evaluated (ion-implanted, substrate fed, up-diffused, p epitaxial, and Schottky). When the variations in isolation and interfacing are added to these, the problem of defining the processing complexity becomes untenable. The problem will not be resolved until many comparable devices are fabricated in each of the major competing LSI technologies so that proper comparisons and evaluations can be made.

SECTION 6

MILITARY SYSTEM REQUIREMENTS FOR LSI DEVICES

One of the objectives of this I^2L technology assessment was to determine the potential uses of I^2L in military systems. The approach taken was to first determine the requirements for LSI devices by surveying Navy, Air Force and Army system program offices and contractors. This information, coupled with the performance and hardening capabilities of I^2L, should lead to a general definition of the application areas for military I^2L LSI devices.

In the military system survey the following areas were addressed:

1. The general functional categories of the electronic subsystems.
2. The maximum desirable level of component complexity to perform these functions.
3. The radiation environments and required levels/goals to which the system will be hardened.
4. Specific LSI circuit requirements and desired performance characteristics.

6.1 NAVY SYSTEM REQUIREMENTS

The major Navy system program office having radiation hardening requirement is the Strategic System Project Office having responsibility for the Poseidon and Trident missile systems as well as development programs such as the Trident II (D5) and Improved Accuracy Program (IAP). One of the major requirements for LSI devices is the guidance computer electronics which constitutes about two-thirds of the missile electronics. Of major interest are the CPU, peripheral and memory circuits as well as dedicated microprocessors for special application. As part of the analysis of I^2L applications for D5, a study was undertaken to determine the system impact of replacing the MSI and discrete components used for driving and reading the plated wire memory system. I^2L LSI parts were considered for replacing the multiplexers, decoders and memory drivers. It was determined that with respect to the IC circuits a 4 to 1 reduction in package count and volume could be achieved along with a substantial reduction in power. However, since most of the total volume and power for the plated wire memory system is consumed by the plated wire stack,

discrete transformers and discrete high current driver transistors, very little would be gained by going to LSI devices. Placing the transformer and high current drivers on the same chip with the digital logic is not feasible. Therefore, if a radiation hardened, non-volatile, fast, static RAM is not available to replace the plated wire memory for missile and satellite computer applications then little can be gained by going to higher levels of integration for the ICs.

An application that would result in a great savings of power, weight and volume (all critical to a missile guidance system) is the remaining portion of the computer. Also if a radiation hardened dedicated microprocessor were available many of the control functions on the gimble assembly could be performed without having to transmit data to and from the computer via slip rings.

In order to determine other Navy system LSI requirements, the results of studies conducted by NAVWPNSUPPCEN Crane and the Naval Avionic Facility, Indianapolis (NAFI) were used. These studies were performed on manned avionic, shipboard and field test equipment to determine circuit function and performance requirements for the Navy's Standard Electronic Module (SEM) program. Although the NAVWPNSUPPCEN/NAFI study did not address Navy systems having a radiation hardening requirement, it helped to identify LSI circuit functions which will have a wide range of application in military systems. The largest category of devices having wide application is that of computer circuits. These circuits have been grouped by function and illustrated in the block diagram of Figure 6.1. Most of these circuits will be developed for commercial computer applications and some are presently on the market in I^2L as indicated in Section 2, e.g., parity generator/checker, microprogram sequencer, 16 bit microprocessor, 4K RAM. The other major function categories of electronic subsystems are data bussing, signal processing, and test/monitor functions. Although in some cases commercial LSI devices may be available which have application in these areas, for the most part these functions will be unique to military systems. Of the circuits that will be used primarily in military applications, and without commercial equivalents, there are two categories of devices:

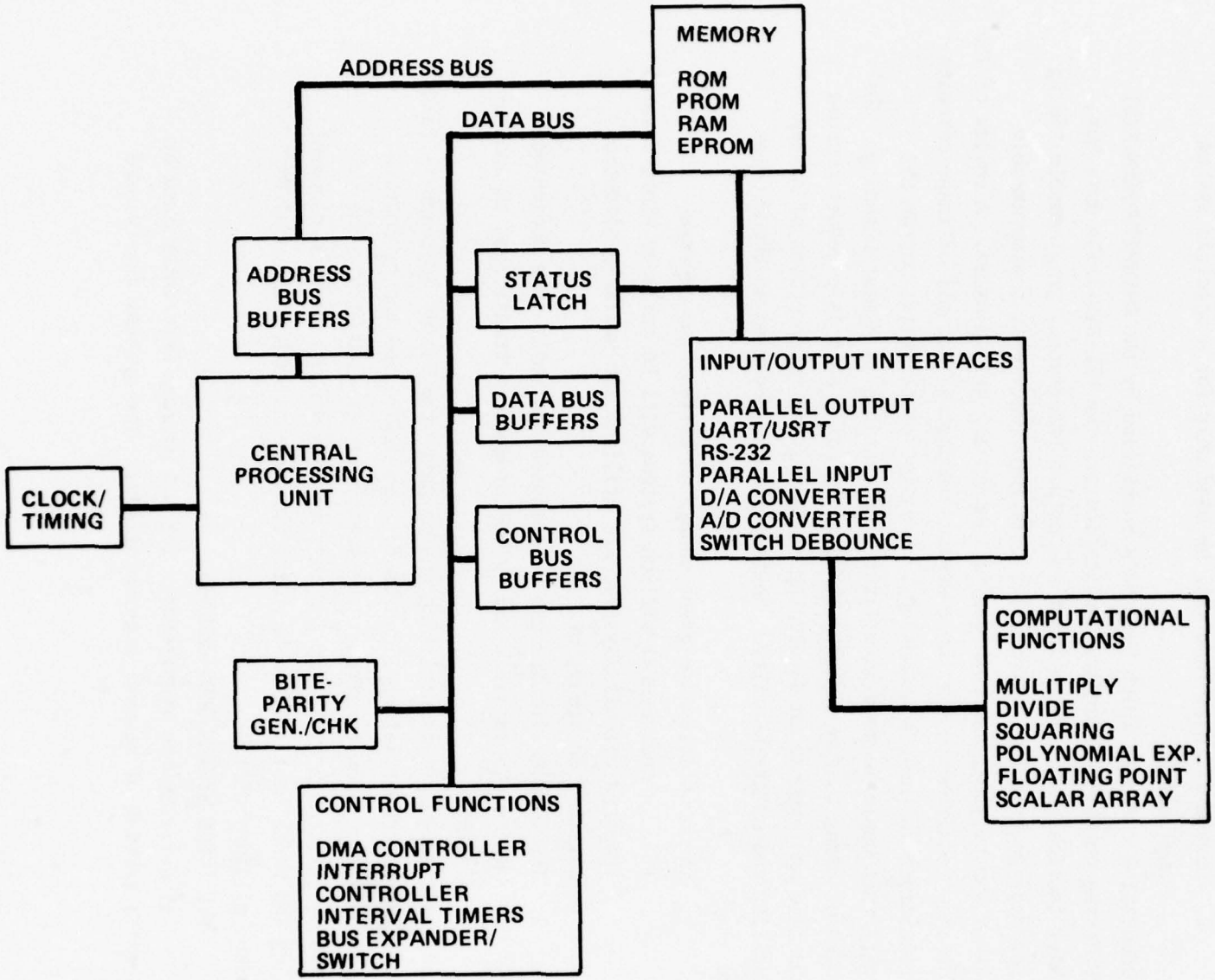


Figure 6.1 Military/Commercial Computer Functions

1. Standard circuits having applications in many different military systems, and
2. Custom circuits that will be used only for a specific system application.

Representative circuits which have been identified by the NAVWPNSUPPCEN/NAFI study having potential standard application are the MIL-STD-1553A data bus, the Navy tactical data system input and output interfaces, programmable timing and sequence generators, Fast Fourier transform functions, a programmable frequency synthesizer, and both digital and analog multiplexers. A review of the performance requirements for these devices indicates that all of these circuits are realizable in the I^2L technology. The list of potential custom LSI circuits that could be used in military applications is almost unending. The approach of using custom circuits is normally taken as a last resort because of the time and expense in developing the parts and the problems of system reliability and maintainability. Custom circuits are used in those cases where

1. The quantities are great enough to warrant the expense, i.e., where several million systems will be built or where several thousand circuits/systems are utilized (an unlikely situation with LSI devices), or
2. The custom circuits can be designed and built in a dedicated system R&D facility and volume production transferred to another facility.

For most military systems utilizing custom parts the latter approach is taken if there is no commercial application for the device and the production quantities are too low to attract the semiconductor industry. The very high volume systems are usually low cost systems without part development funding and hence must rely on building the systems with commercial or standard military parts.

6.2 AIR FORCE SYSTEM REQUIREMENTS

Air Force System requirements for LSI devices were determined by personal interview of several program offices. The systems interviewed

for this study were the Defense Systems Communications Satellite System (DSCS), the Global Positioning Satelite System (GPS), the Air Force Satellite Communications Systems (AFSATCOM), Defense Satellite Program (DSP), Defense Meteorological Satellite Program (DMSP), and several potential subsystems of the MX missile system.

Satellite requirements are somewhat unique in that the number of semiconductor devices are few in number, require a very high degree of reliability, and must be hardened to a natural radiation environment independent of the hostile threat hardening requirement. This implies a minimum risk approach to the electronics. Therefore, the opinion was expressed by several of the satellite program offices that only commercially available, proven reliable, low risk technology parts will be used. Part of the drive toward commercial parts is also due to the lack of both lead time and money to develop custom parts for systems. While this was the opinion of most system offices, one exception was AFSATCOM which has longer lead times for the second and third phase systems. Although consideration is being given for several custom LSI devices the design criterion will be met with commercially available parts. The DMSP system, while utilizing commercial bulk CMOS part types, has undergone a program to harden parts for ionizing radiation.

In addition to the satellite systems offices, the MX program office was surveyed to determine hardened LSI circuit requirements for Air Force missile systems. The MX program office has several feasibility and design/prototype efforts in progress for different subsystems of the MX missile. These subsystems include the stable platform, the guidance computer, the re-entry system, as well as launch and ground support subsystems. Therefore, the total system is multifaced with a variety of performance and hardness requirements. The schedule of operational systems will have a direct impact on the technology approach taken for the design and implementation of electronics. If a state-of-the-art technology approach is taken then a significant number of LSI devices will be used in the missile and guidance electronics. The less critical (in terms of radiation hardening) launch and ground support systems will use commercially

available parts rather than go through a components developmental program. At this point in time, commercial I^2L LSI circuits could be considered for MX ground support systems if radiation characterization of candidate parts indicates adequate hardness.

6.3 ARMY SYSTEM REQUIREMENTS

In an attempt to get a response from many Army system program offices, a written questionnaire was prepared and mailed to all program offices within the Army Material Command. Of the 60 questionnaires mailed, about 30 were returned. Only five program offices indicated there was a radiation hardening requirement on their system and ten indicated they would use LSI devices. The most frequently mentioned desirable LSI circuits were microprocessors and memories. Two systems will utilize custom LSI circuits. The remaining 20 responses to the survey indicated that the highest level of component complexity would be either SSI or MSI devices. Most Army systems are constrained to use commercially available parts. For such systems the major impact of I^2L will be in the computer, signal processing, and combined analog/digital areas.

6.4 MILITARY SYSTEM REQUIREMENTS DETERMINED FROM SYSTEM CONTRACTORS AND DESIGN AGENCIES

Although the primary approach to system survey was to contact the military program offices, several system contractors and design agencies were also surveyed. Among those queried about their requirements for hardened LSI electronics were Sandia Labs, General Electric, Northrop, Raytheon, Autonetics, Hughes, and Charles Stark Draper Labs. All of these companies have programs related to many different military systems for which the company, as a whole, attempts to take a unified approach to LSI. At least five of the companies have their own LSI design and fabrication laboratories which are used for custom LSI design. Of the five R&D laboratory facilities mentioned, three (Northrop, G.E. and Hughes) have ongoing efforts in custom I^2L LSI. None of these efforts is of the magnitude of the similar programs in bulk CMOS and CMOS/SOS. This is due primarily to the fact that I^2L is a much more recent technology.

The information obtained from these companies concerning the requirements for LSI devices was consistent with information from the program offices, the major areas of concern being in computer applications, signal processing, data bussing, interfacing, and analog/digital converters.

As with the program office survey, the company survey did not yield much information on actual circuit and performance parameter requirements. Specific LSI circuits that were mentioned as being considered for use in military systems fell into the following categories: microprocessors, static RAMs, ROMs, correlators, transforms, counters, data buses, voltage comparators, time base generators, successive approximation registers, and regulator/modulator/sequencer control circuits. In addition many custom LSI parts used for a specific system application are being designed and fabricated in the system contractor R&D labs.

As a part of the survey the company individuals were asked for their opinions concerning the use of I^2L LSI devices in military systems. Although most responses were very positive about the potential of I^2L, the major reservations concerned the unproven speed to handle real time processing for such applications such as radar, the lack of commercially available I^2L circuits, the problem of proper interfacing for military applications, and the unproven radiation hardness.

6.5 SUMMARY

Responses to the four areas addressed in the military system survey are summarized in the following paragraphs.

a. Functional Categories of Electronics. The major category of military electronics can be lumped under computers. This category includes all of the function shown in the block diagram of Figure 6.1. Another large category is digital signal processing. This area includes such functions as correlators, convolvers, filters, frequency synthesizers, multipliers, and transforms. Other categories identified in the survey are data busing, coding, A-D and D-A conversion, and test/monitor functions. Although the list is far from comprehensive it represents a major portion of military electronics.

b. Maximum Level of Component Complexity That the Systems Will Use. This question involves a tradeoff between such variables as reliability, testability, component cost, performance parameters, system constraints (such as size, weight,and power), limitations in hardware and software flexibility, hardening and maintainability. One of the major considerations which affects component cost, and maintainability is the commercial or MIL-STD availability of parts. Using off-the-shelf or MIL-STD-38510 devices is generally a constraint placed on high volume, low cost systems. This includes many Army systems.

The advantages to be gained in going to LSI devices are lower power, weight and size and lower failure rates due to the reduction in piece part count and interconnects. In most cases there is also a significant reduction in cost per function unless the circuits are low volume custom parts with high development costs. For most systems, the highest level of complexity will be used if the required circuits are commercially available and the use of such devices results in overall system cost reduction. There are, however, many high performance systems (satellites, missiles, and avionic systems) for which performance, size, power, reliability, and hardening are the major considerations and the component costs are secondary. These systems will use LSI devices regardless of the development and piece part cost if the devices offer significant advantages in performance and can be demonstrated to have the necessary reliability and hardness.

c. Radiation Environments. Information about the radiation environments and levels was obtained from each of the systems requiring radiation hardening. These levels range from quite modest to very demanding. Specific requirements are well known and should be discussed with a specific project office or DNA.

d. Specific LSI Circuits and Performance Parameters. This information was sought for two reasons.

1. To project the potential use of I^2L for specific systems applications based on the requirements for speed, drive capability, power dissipation, etc.
2. To identify a widely used LSI circuit that could be used as a demonstration vehicle for a radiation hardened I^2L program.

No consensus of opinion was obtained on either point during the course of this study. Although most new system designs push the state-of-the-art in overall system performance, it does not follow that state-of-the-art semiconductor devices are used to meet the system requirements. There are usually many alternative designs utilizing different levels of component performance and complexity. Therefore the choice of components is usually based on what is available to the design engineer either commercially or through the MIL-STD system.

Because the military part of the semiconductor market is only a small percentage of the total market, military applications are not the driving force. Therefore system designers tend to adapt to commercially available parts to implement system functions if possible. Only in those instances where system performance requirements cannot be met with commercial parts is there incentive to carefully describe in detail the piece part performance requirements. Such requirements are generally not specified until advanced stages of design and prototyping of the system. Therefore, the only specific information about LSI piecepart performance requirements was in the form of specifications for custom LSI devices developed for a system. In these cases the technology and design had already been selected.

SECTION 7

CONCLUSIONS

I^2L is a rapidly developing technology with much promise for radiation hardened LSI arrays. The major effort in I^2L development is for low power, high density, high speed computer applications. This has brought about changes in the basic inverter cell design which have significantly increased the neutron and total dose hardness over that of baseline or first generation I^2L. Although preliminary neutron and total dose test data on several of the second generation structures indicate that simple inverter cells, ring oscillators, flip flops, etc., can be fabricated with good electrical performance and radiation hardness, very few actual LSI circuits have been produced using these structures. Production of LSI devices with reasonable performance, reliability, and yield is a very difficult problem with any technology. One major advantage that I^2L offers is simplicity in processing. While this is true for the baseline process, propagation delays limit its application. Emerging second generation structures, while not introducing many additional processing steps, require significant alterations to conventional bipolar processing as well as tighter controls. Such processes as up-diffusions, double epitaxy, double diffusions thru the same oxide cut, deep implantations, and various forms of oxide isolation are significant departures from the simple baseline process. The structure representing the least departure from the baseline process, i.e., the ion-implanted structure, is the only one that has been realized in an actual product (T.I.'s SBP9900 and Fairchild's 9408). The other structures are unproven at the LSI level. This means that much work remains in terms of optimum design and layout for packing density, process controls to achieve geometric and profile tolerance over large chip areas, injector rail design to minimize IR drops, interfacing schemes, isolation schemes, and other problems which will arise when the circuit complexity is extended.

In order to assure that changes which are introduced to increase performance, yield, cost, packing density, etc., do not adversely affect radiation performance, an understanding of the radiation damage mechanisms and the variables which affect hardness is essential. Although a reasonable understanding of the neutron and total dose damage mechanisms in I^2L exists, dose rate upset has not been addressed to a great extent. A better understanding of dose rate upset mechanisms in

simple I^2L circuits as well as understanding of the interaction between adjacent or electrically connected gates in an array is required in order to design large arrays with optimized dose rate hardness. Since optimum performance, packing density and yield can be achieved on the simpler non-isolated form of I^2L, work should be done to improve the I^2L I/O structures to increase the tolerance to electrical pulse overstress and noise immunity. If reasonable tolerance to these environments is not possible with pure I^2L forms, then properly designed I^2L buffering will have to be used. Characterization of I^2L test structures and devices should continue for neutron, total dose and dose rate effects. The data taken to date has been quite limited and has only included one complete LSI device. No data has been taken on isolated I^2L forms, either T^2L interfaced digital arrays, or combined analog/digital circuits. Second generation I^2L structures have not been measured for dose rate upset and very little data exists on the injection level dependence of dose rate effects. Although it can be assumed that the transient annealing of gain degradation in I^2L devices from a pulsed neutron environment is similar to the effect in other bipolar devices, no data has been taken to measure the effect.

In the military systems analysis for hardened LSI requirements the major functional category identified for LSI devices is the computer area. The development of a radiation hardened I^2L computer chip would therefore have an immediate impact for many military systems. There seems to be little agreement, however, on the approach to building military computers using LSI devices. Many designers prefer using a dedicated microprocessor approach whereas others prefer the more flexible bit slice approach. With either approach, however, certain peripherals such as memories, computational functions, data busses, control functions, etc. are required. Therefore the development of a radiation hardened I^2L peripheral computer chip may find wide acceptance. Such a device would not only be a useful part for actual systems applications but could be used as a demonstration vehicle to explore the potential radiation hardening of a second generation I^2L process. In demonstrating the feasibility of producing a radiation hardened LSI I^2L device, the tradeoffs of hardening vs. yield and performance can be explored. These should include not only inverter cell geometry and profile tradeoffs, but circuit layout schemes, photocurrent compensation, isolation techniques, and I/O interfacing circuits. A full radiation effects characterization study on the demonstration circuits should include long term neutron and ionization effects, dose rate upset and survivability,

transient annealing from neutron pulses and electrical pulse overstress burnout thresholds. The information derived from such a study could be used define guidelines for the design and processing of radiation hardened I^2L arrays. These guidelines could then be used to aid in the layout and fabrication of other standard military LSI devices as well as custom circuits.

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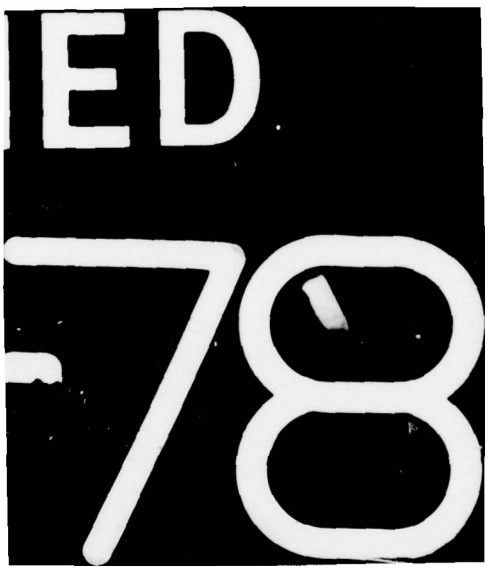
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